ELECTRONIC RECORDING PRODUCTS

Instructions

RADIO CORPORATION OF AMERICA,
Broadcast and Communications Products

MAINTENANCE

TR-22 Television Tape Recorder

SERVO SYSTEMS

Tmk(s) ®

IB-31622

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Outside of Continental United States, Alaska, Hawaii and the Dominion of Canada	RCA International Division, Clark, N. J., U.S.A. or through your local Sales Representative.

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Portland 12, Oregon
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Memphis, Tenn.
3189 Summer Ave.
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Seattle 4, Washington
2250 First Ave., S.
MAin 2-8350

Washington 6, D. C.
1725 K St., N.W.
FEderal 7-8500

West Palm Beach, Fla.
645 S. Military Trail
683-2219

ELECTRONIC RECORDING PRODUCTS

MAINTENANCE

TR-22 Television Tape Recorder

SERVO SYSTEMS

RADIO CORPORATION OF AMERICA
BROADCAST AND COMMUNICATIONS PRODUCTS, CAMDEN, N. J.
PRINTED IN U. S. A.
IB-31622
GO 634

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

HEADWHEEL SERVO

SYSTEMS DESCRIPTION

GENERAL

The headwheel servo system of the TR-22 Television Tape Recorder includes the following modules:

Reference Generator (no. 312)
Tonewheel Processor (no. 313)
Tonewheel Servo (no. 314)
Headwheel Modulator (no. 315)
Linelock (no. 316)
Tape Sync Processor (no. 317)
Power Amplifiers (nos. 332, 333, 334)

If the machine is to be operated on International standards, the International version of the reference generator and tape sync processor modules must be incorporated into the headwheel servo system. All other modules function properly on either domestic or International standards.

The purpose of the headwheel servo system is to control the headwheel motor speed during both the tape recording and the tape playback processes. In either the RECORD or PLAY mode, the nominal speed of the headwheel motor is 240 rps; however, it is desired to exercise very tight control over this speed for reasons which are explained below.

NOTE: Throughout the following discussion of the headwheel servo system, timing references in text and illustrations pertain to 525-line, 60-cycle, domestic standards. When dealing with International (50-cycle) standards, the appropriate timing differences must be taken into consideration; e.g., the 240-cycle tonewheel pulse becomes 250-cycle, etc.

RECORD Mode

In the RECORD mode, it is desirable to attain a headwheel motor speed in revolutions per second which is exactly equal to four times the vertical scanning frequency; i.e., 240 cps. Because the timing reference for the television system may be derived from any one of several sources, the most practical method of controlling the headwheel speed is by utilizing a servo system in which an error detector compares the frequency and phase of a signal developed by the tonewheel attached to the headwheel motor shaft against a reference pulse derived from the signal itself. This action assures that each television field period occupies exactly sixteen complete transverse tracks on the tape. (Note that each revolution of the headwheel produces four tracks because of the four video magnetic heads equally spaced around the headwheel circumference.)

If the headwheel motor speed were fixed at 240 cps during recording, with no direct comparison to the vertical scanning frequency, the relative phase of the television signal as laid down on the tracks would tend to drift slowly in one direction or the other. For example, the first vertical sync pulse in each field would occur sometimes near the center of the tape, and sometimes near the edge of the tape where the head switching action occurs. In addition, the 60-cycle pulse applied to the control track as a means of identifying the beginning of each field for tape splicing purposes would tend to drift in phase relative to the 240-cycle sinusoidal control track signal. While an individual machine could be made to operate effectively with such a condition of relative drift (provided no attempt is made to play back a tape that has been spliced after recording), the practical problems associated with tape splicing and the interchangeability of tapes between machines make it important that the headwheel speed be closely controlled relative to the scanning frequencies.

Figure 1 is a simplified block diagram of the headwheel servo system during recording. The 480-cycle motor drive sine wave, locked in phase to the tonewheel pulse, is developed from the output of an afc circuit. The sine wave is split into three individual sinusoidal signals which are separated in phase by 120 degrees, amplitude modulated, and fed to power amplifiers. The power amplifiers in turn drive the three-phase synchronous headwheel motor.

Amplitude modulation of the motor drive sine wave is controlled by: (1) a comparison of the tonewheel pulse phase with a fixed reference signal to obtain phase information, and (2) a comparison of the tonewheel pulse period with a fixed time interval to obtain velocity information. (In the RECORD mode the fixed reference signal may either be sync from the incoming video signal, or the signal from an external sync generator or oscillator.) The error signals derived from the phase and frequency comparisons are added in such a manner as to cause the velocity error signal to predominate when large errors occur (e.g. during headwheel motor start-up when the phase is changing rapidly), and the phase error signal to predominate when the motor is at approximately the correct speed with only slight variations in phase.

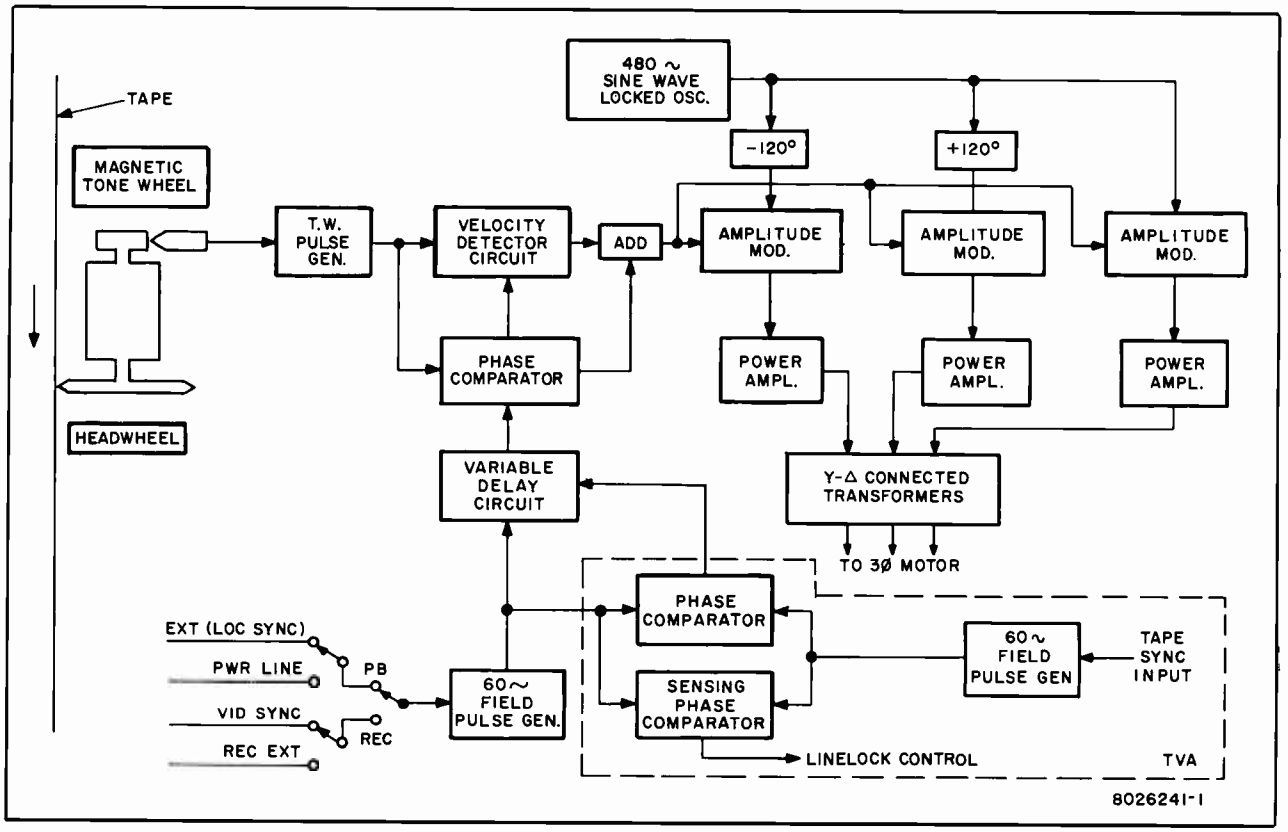


Figure 1—Simplified Block Diagram of Headwheel Servo in Tonewheel Mode with TVA

The motor drive signals are pulse modulated at a line frequency rate (15,750 cps) by chopper circuits, and the width of the modulating pulse is controlled by the combined error signal referred to above. Thus the energy contained in each sinusoidal signal will be proportional to the error signal amplitude. The line frequency information is then filtered out, thus leaving the fundamental 480-cycle sine wave signal whose amplitude is a function of the energy remaining after modulation.

NOTE: In International machines the line rate, and thus the modulating pulse frequency, depends upon the line standard in use. Headwheel servo modules in the International machines are wired for one of two line rate sequences. These are either the 405/525/625 standards or the 525/625/819 standards.

The tape vertical alignment (TVA) circuit shown within the dashed lines in figure 1 has no function during recording or during tape playback in the tonewheel servo mode. However, the TVA circuit does produce an output control voltage during these modes which converts the variable delay in the reference pulse path into a conventional emitter follower. This action eliminates the delay, which is utilized only during tape playback in the pixlock servo mode as will be explained later.

PLAY Mode

Tonewheel and Switchlock Servo Modes

During tape playback, provision is made to operate the TR-22 Television Tape Recorder servo system in the tonewheel, switchlock, or pixlock mode. These modes constitute increasingly greater control of tape to reference vertical and horizontal sync timing as the machine is switched from tonewheel to switchlock to pixlock mode. The function selector switch, by which the operator may select the desired mode, is located on the tape sync processor module (no. 317) front panel. The actual choice of modes selected depends upon the degree of timing control required to perform a certain operation; however, it should be noted that to successfully play back tape in the pixlock servo mode the tape must be of good broadcast quality (i.e., a tape containing clean sync signals, without dropouts or other forms of discontinuity).

Normally, satisfactory performance will be attained when tape is played back with the servo system operating in the tonewheel mode. In this mode no attempt

is made to align tape and reference vertical sync, and the headwheel motor speed is controlled by the tonewheel pulse in exactly the same manner as that described above for the RECORD mode (see figure 1). The choice of servo reference during tape playback in the tonewheel mode is either a signal from an external sync generator or oscillator, or the power line frequency.

If it is desired to attain vertical framing so that vertical rollover of the picture is prevented when switching between tape and other program sources, the servo system must be operated in the switchlock mode. In this case the headwheel servo remains in the tonewheel mode, while the capstan servo operates in the switchlock mode to control the tape speed and vertical sync phasing to achieve vertical framing. Operation of the machine in the switchlock servo mode is explained in greater detail below during the pixlock servo discussion. (Refer also to the *Capstan Servo System* description.)

Pixlock Servo System

The function of the pixlock servo system is to accurately synchronize vertical and horizontal sync pulses derived from television tape signals with vertical and horizontal sync pulses provided by the station's local sync generator. This allows an extension to tape television signals of the lap dissolve, special effects, and other types of transition currently employed between two or more live or film television signals.

The pixlock servo system is actually a combination of the switchlock and linelock servo systems. Briefly, the switchlock system operates independently of the linelock system, and its function is to control the capstan servo so that the speed of the tape and phase of the tape vertical sync is such that vertical rollover of the picture is prevented when switching between tape and other program sources. The linelock system, however, operates in conjunction with the switchlock system in providing accurate control of the headwheel motor speed to maintain a precise relationship between tape and local horizontal sync pulses, thus insuring that the tape system is completely locked both vertically and horizontally.

The operation of the pixlock system in lining up vertical and horizontal sync from television tape signals with the local station sync pulses may be divided into four distinct phases which automatically occur in sequence. Phases one and two are performed by the switchlock servo while phases three and four are performed by the linelock servo. In the pixlock system, the time required to complete all four phases is less than five seconds from the moment the PLAY pushbutton is pressed for tape playback in the pixlock mode. The pixlock functions are completely automatic so that if there are any discontinuities in the tape signal or reference signal while playing back tape, the machine will go through only the necessary operations to re-synchronize, taking a total time of three seconds or less.

The first phase of operation begins when the machine is signalled to start in the PLAY mode. Capstan and headwheel motor power are immediately switched on and the motors are accelerated to their correct operating speeds so that a stable picture signal is played back from the tape. Once a picture signal is received, the machine begins the second phase of operation, designated "coarse vertical framing." In this operation the machine shifts video tracks until it plays back the recorded track containing vertical sync at the same time as the local vertical sync is occurring. This operation does not provide exact vertical framing however, because it does not compensate for errors of placement of vertical sync in the recorded pattern on the tape. To compensate for these errors the machine enters the third phase of operation, designated tape vertical alignment (TVA). Here the tape and local vertical sync signals are accurately compared and the necessary slight adjustment of the headwheel phase is introduced, resulting in "fine vertical framing."

At this point the picture signal from the tape will be timed to within a few microseconds of its correct position, and will be moving several microseconds left and right of this position. The motion results because the information fed to the servo occurs at too slow a rate (60 samples per second) to allow for complete correction. The fixed error is present because the loop gain cannot be made large enough, at a low sampling rate, to reduce the error further.

When the machine senses that the TVA cycle has been completed, it switches into the final or "linelock" phase of operation. In the linelock mode, the headwheel servo is controlled by comparison of horizontal sync from the tape signal with the local horizontal sync. Error information is thus provided at a suf-

ficiently high rate that the servo gain is readily increased to overcome much more rapidly varying errors.

The following discussion presents a more detailed explanation of the four phases of pixlock operation in terms of the servos themselves. The first phase (headwheel and capstan motor acceleration) is accomplished with the headwheel servo operating from the tonewheel and the capstan servo operating from the control track. This is primarily the same operation as the tonewheel mode, however the TVA circuit is actually in the headwheel servo loop although it does not furnish any additional information in the first phase of the pixlock sequence.

In the TVA tonewheel mode, the magnetic tonewheel head delivers one pulse for each rotation of the headwheel. After passing through shaping circuits, the 240-cycle pulse obtained from the tonewheel is fed to a velocity detector circuit and to a phase comparator as shown in figure 1. The velocity detector circuit produces a d-c voltage which is a function of the period between pulses, and this error voltage feeds the modulator which modulates a three-phase 480-cycle sinusoidal signal. The output of the modulator feeds three power amplifiers, and Y — Δ connected transformers drive the three-phase induction headwheel motor.

When the headwheel motor is started from rest, the velocity error voltage fed to the modulator causes full power to be delivered to the motor so that it will accelerate as fast as possible. As the headwheel motor speed approaches 240 rps, the error voltage is reduced and less power is delivered to the motor by the modulator, thereby resulting in rapid headwheel speed stabilization. At this point the phase error voltage, obtained from the phase comparator circuitry, assumes control of the headwheel motor speed. This voltage is a function of the phase relationship between the tonewheel pulse and a 60-cycle pulse derived from local vertical sync. The servo loop controls the headwheel motor so that these pulses are locked together.

In this servo, the motor drive voltage responds very rapidly to error voltages because phase shifting is accomplished before modulation and very little filtering or wave shaping is required in the channels which follow the modulator. Also, the 480-cycle motor drive frequency is derived from an oscillator which locks at exactly twice the tonewheel frequency, thereby eliminating any beats which would be caused by a free-running motor drive frequency. These features greatly increase the accuracy of the tonewheel servo, thereby minimizing recorded servo error or jitter.

When the capstan and headwheel motors have come up to speed and have locked-in in their normal modes, a video signal becomes available from the tape being played back and the machine enters the second phase of operation (coarse vertical phasing). This phase of operation takes place wholly within the capstan servo while the headwheel servo continues to operate from the TVA tonewheel. The action here consists of the capstan servo looking at the frame information played back from the tape, and "slipping tracks" until this frame information matches frame information derived from the local sync signals. A 30-cycle frame pulse is formed from the tape sync signal input by a circuit similar to that used in deriving a frame pulse from local sync. The tape frame pulse thus formed is then injected into the capstan servo system as a reset pulse to accomplish framing.

The third phase of system operation consists of compensating for errors which exist between the local and tape vertical sync signals because of placement errors of the recorded vertical sync in its track. This compensation is provided by the TVA function of the system.

Basically, the TVA circuit directly compares vertical sync, or field pulses, derived from the tape and from the local signals. The comparator output (a d-c voltage) controls a variable delay circuit which has been added in the 60-cycle reference input path of the headwheel servo (figure 1). The delay circuit adjusts the apparent phase of the 60-cycle reference, thereby controlling the rotational phase of the headwheel. By this means the TVA variable delay circuit can make small adjustments of headwheel phase to shift the phase of the tape playback signal. The TVA loop has a very high gain, so that the resultant error when it stabilizes will be small; however, the loop is deliberately designed to be slow-acting so that it does not interfere with the normal start-up and lock-in of the headwheel servo. TVA comes into action only after the main servo has locked-in and the capstan phasing cycle has been completed, because prior to this there is either no signal from the tape or the framing is so

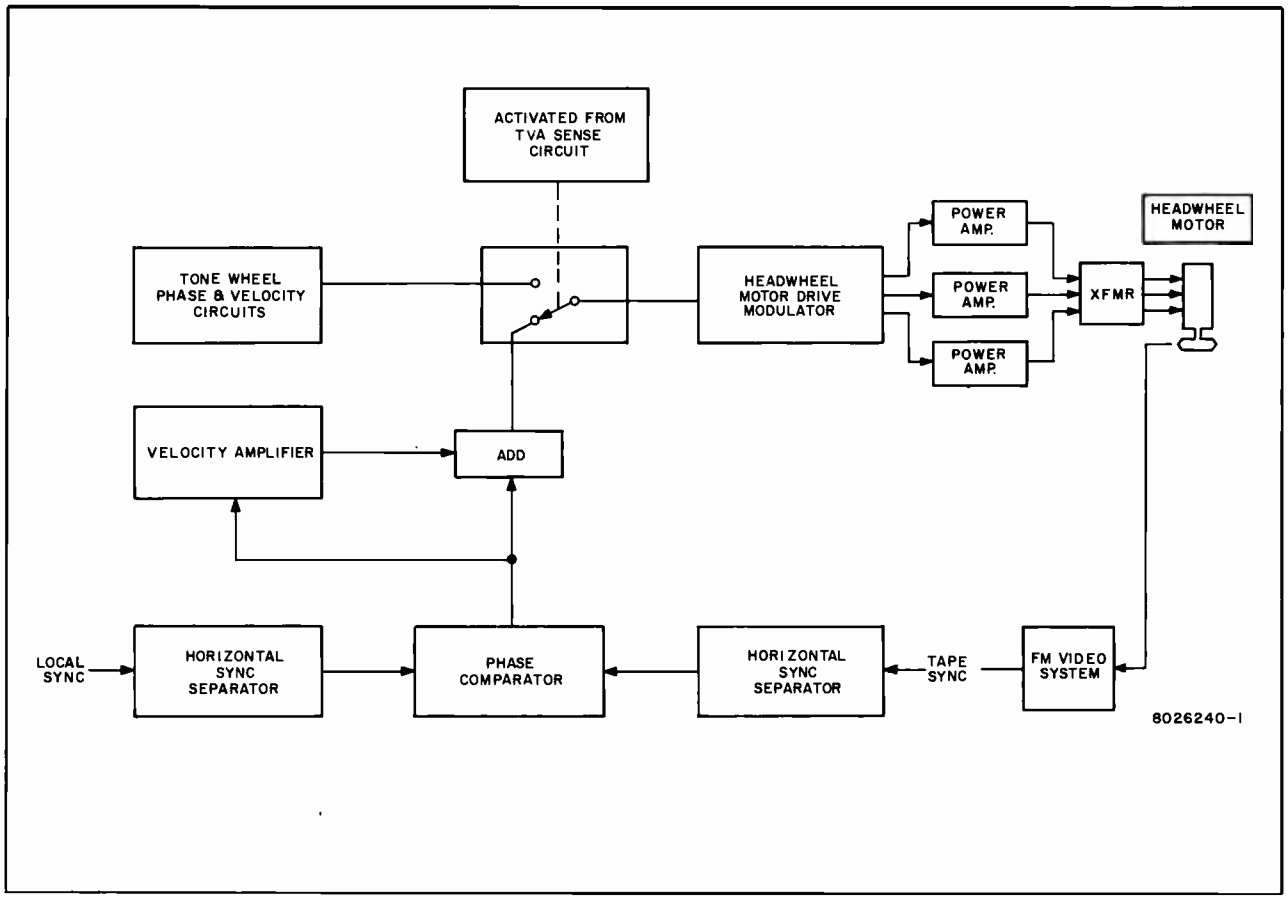


Figure 2—Simplified Block Diagram of Headwheel Servo in Linelock Mode

far off that the TVA phase comparator is outside of its useful range.

A coincidence circuit is used as a sensing device which indicates when the TVA circuits have stabilized at their correct phase. This circuit provides an output signal only when the local and tape vertical sync signals are within a few microseconds of each other. The presence of the sensing signal causes the pixlock servo to automatically switch to the fourth (linelock) phase of operation.

Figure 2 is the block diagram of the pixlock servo in the linelock mode. The input to the headwheel motor drive modulator is electronically switched by the TVA sense circuit from the tonewheel phase and velocity circuits to the linelock circuits. These circuits include a phase comparator which compares tape and local horizontal sync signals. The d-c error signal thus derived is fed to the headwheel motor drive modulator by two paths. The first path is direct; the second path passes the signal through a velocity amplifier circuit whose purpose is to provide a stabilizing function in the loop, thus allowing higher loop gain without overshoot or oscillation.

Control of the headwheel motor speed by the linelock loop is limited only by the power capabilities of the motor drive system. The gain and response speed are sufficiently high that the maximum phase error between local and tape sync signals is less than ± 0.1 microsecond when playing back a tape which was recorded with a pixlock servo system.

It should be recognized that the performance of the pixlock system is a function of both the recording and the playback equipments. Therefore, the jitter of the recording is very important, and for best stability tapes should be recorded by a low jitter recording servo system such as is provided by the pixlock system itself. Recordings made with other servo systems may contain excessive jitter which is not of great importance during conventional playback, but which may be very detrimental when trying to achieve precise control of the headwheel motor by the pixlock servo operating in the pixlock mode.

HEADWHEEL SERVO SETUP PROCEDURE

The setup procedure outlined below is intended as a guide in making rapid checks and minor adjustments which insure optimum headwheel servo performance. All waveforms specified may be monitored directly on the machine, and therefore no external test equipment is necessary. Detailed procedures for making each adjustment in the headwheel servo system according to the various modules are presented in the *Adjustment* section of the individual module descriptions, and should be referred to when setting up the servo initially and when module or component replacement necessitate complete re-adjustment.

Head Select Operation

1. Depress the VID IN and DEMOD OUT pushbuttons on the CRO monitor switcher simultaneously, and also depress the EXT SYNC pushbutton.

2. Depress the V and EXP pushbuttons located along the right-hand edge of the CRO monitor.

3. Play back a tape in the switchlock servo mode and switch from head no. 1 to head no. 4 (utilizing the HEAD SELECT switch on the reference generator module, no. 312) while noting the tape vertical sync displacement on the CRO monitor at each position of the switch.

4. With switch position no. 1 as a reference, the displacement of tape vertical sync should not exceed three-fourths of a horizontal line in any of the remaining switch positions. If the maximum displacement is exceeded, re-adjust potentiometer R54 to obtain a minimum displacement.

Velocity Time Constant

1. Play back a tape, using the EXT SERVO reference, and operate the picture monitor on external sync.

2. Press the VEL TC button on the tonewheel servo module (no. 314), and observe the picture on the monitor.

3. If horizontal roll-through occurs, re-adjust the VEL TC potentiometer on the tonewheel servo module to minimize the roll-through. (Adjust the potentiometer in the clockwise direction to stop the picture from rolling to the left, and adjust the potentiometer in the counterclockwise direction to stop the picture from rolling to the right.)

4XTW DELAY

1. Play back a tape and observe the picture monitor to detect the presence of 960-cycle streaks which may enter the picture from either the left or the right side.

2. If streaks are present, adjust the 4XTW DELAY potentiometer on the tonewheel processor module (no. 313) so that the potentiometer is centered in the range over which no streaks appear.

FM Switching

1. Play back a tape in the tonewheel servo mode, using EXT servo reference.

2. Operate the picture monitor on EXT sync.

3. Utilizing the HEAD SELECT switch on the reference generator module front panel, select the head which allows the horizontal blanking and sync pulse to be observed.

4. Operate the guide servo manually and, utilizing the PB GUIDE POSITIONING control on the guide servo module (no. 221), decrease tip penetration slightly to emphasize switching dots. (Adjust picture monitor brightness and contrast to obtain best results.)

5. Correct switching is indicated when the switching dots are located within the horizontal sync interval, and approximately one-third in from the leading edge of sync. If necessary, adjust the TAPE HOR FREQ SET potentiometer on the tape sync processor module (no. 317) to properly position the switching dots.

Tonewheel Servo Gains

The VEL GAIN and PHASE GAIN potentiometers on the tonewheel servo module (no. 314) generally require re-adjustment only when the headwheel panel is replaced.

Linelock Servo Gains

Because the linelock servo utilizes the tape signal in obtaining some of its information, the VEL GAIN and PHASE GAIN potentiometers on the linelock module (no. 316) may require re-adjustment when certain tapes are played back. If re-adjustment is required, it will be necessary to follow the procedure outlined in the linelock module description.

It should be noted that optimum results during tape playback will be obtained from tapes which have a minimum of recorded jitter. Therefore, for maximum stability during tape playback tapes should be recorded by a low-jitter recording servo system such as that provided by the pixlock system itself. Recordings made with other servo systems may contain excessive jitter which is not of great importance during conventional (tonewheel) playback, but which may be detrimental when attempting to achieve precise control of the headwheel motor speed by operating the machine in the pixlock servo mode.

MODULE CIRCUIT ANALYSES

In the following analyses of the individual modules which are contained in the headwheel servo system, timing references pertain to domestic standards; i.e., a 15,750 cps horizontal rate (525-line) and a 60-cycle field rate. A special reference generator and tape sync processor module (nos. 312 and 317) will be utilized in the International machines to accommodate International line standards and a 50-cycle field rate. The description of each of these modules is presented separately, following the domestic module description. The remaining headwheel servo modules contain circuitry which allows them to operate efficiently in either domestic or International machines.

Partial schematic diagrams are intended to show only the area under discussion. For a complete schematic diagram refer to the *TR-22 TV Tape Recorder Diagram Manual,* IB-31616. A functional diagram of the headwheel servo system (figure 125) and a diagram of controls and indicators (figure 124) will be found at the rear of this instruction book. These diagrams are provided as aids in obtaining an overall conception of the function of the circuits which make up the modular portion of the headwheel servo system.

REFERENCE GENERATOR MODULE (DOMESTIC)

Circuit Description

General

The function of the reference generator module (no. 312) is to produce five individual output signals for use in the headwheel servo, capstan servo, and monitoring subsystems, from any one of four input reference signals. (See block diagram, figure 3.) The output signals and their destinations are as follows:

1. Reference horizontal sync to the CRO and picture monitors for synchronizing the monitors.

2. Vertical sync to the capstan servo subsystem where it is used in developing the reference frame pulse.

3. Phase sample pulse (derived from reference vertical sync) to the headwheel servo subsystem for phase control of the headwheel motor in tonewheel or switchlock modes during playback, or tonewheel mode when recording.

4. Reference vertical sync to the headwheel servo subsystem for tape vertical alignment (TVA) control in the pixlock mode of operation during playback; and to the reference pulse switch position (REF PULSE) of the CRO monitor switcher for monitoring purposes.

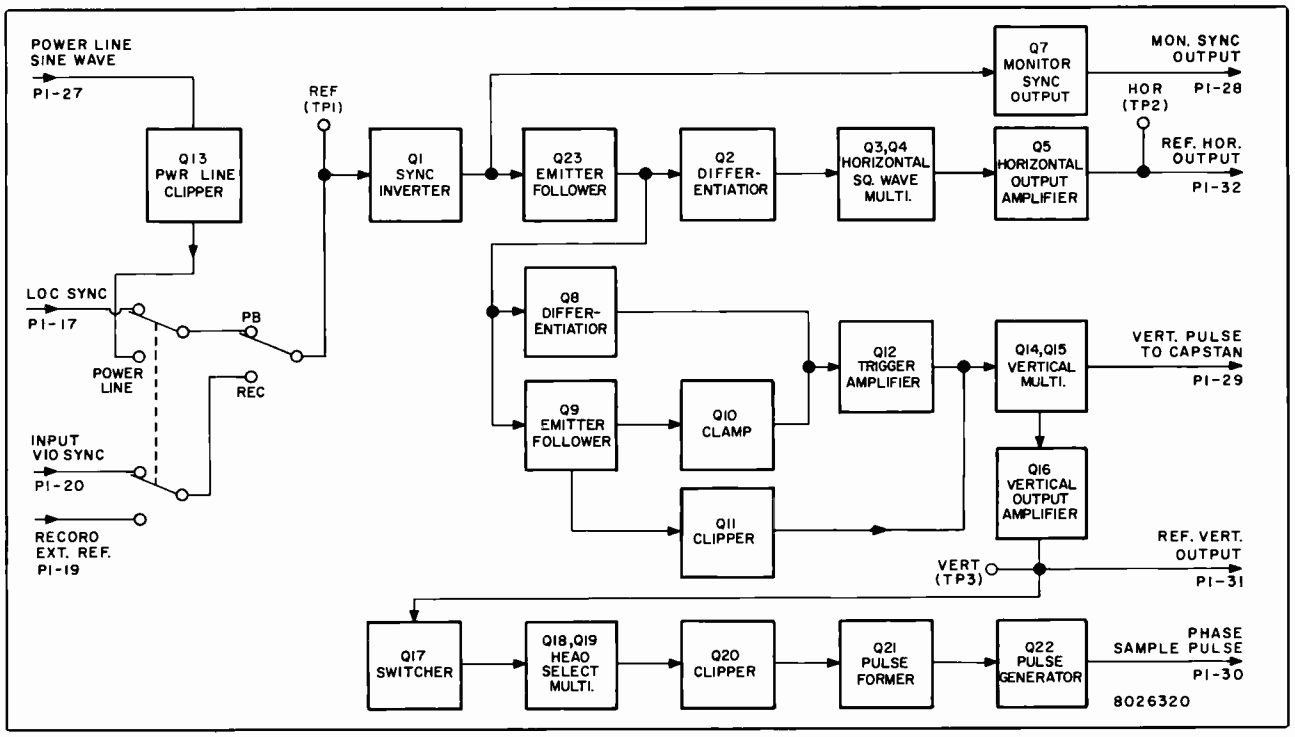


Figure 3—Reference Generator Module Block Diagram

5. Reference horizontal sync to the headwheel servo subsystem for speed and phase control of the headwheel motor on a line-for-line basis in the pixlock mode during playback; and to the capstan servo subsystem where it is used in developing the reference frame pulse.

The input signals to the reference generator are determined by the operating mode of the machine (RECORD or PLAY), and two choices of reference are available for each mode. The input signals to the reference generator are:

1. Local sync or power line reference, which may be selected for system reference during playback by means of a pushbutton on the PLAY control panel.

2. Video sync or record external reference sync, which may be selected for system reference when recording by means of a pushbutton on the RECORD control panel.

Reference Horizontal and Monitor Sync Pulse Generator

Relay K1 (REC/PB) is deenergized when the tape recorder is operated in the PLAY mode (figure 4). The input reference signal is then selected by relay K2 (REF SELECT RLY), and the choices available are local sync (when K2 is deenergized) and power line (when K2 is energized). The condition of relay K2 during playback is controlled by the SERVO REF pushbutton on the PLAY control panel. Similarly, two input reference signals are available when the tape recorder is operated in the RECORD mode. In this mode relay K1 is energized, and the input signals available are video sync (when K2 is deenergized) and record external reference sync (when K2 is energized). The condition of relay K2 when recording is controlled by the SERVO REF pushbutton on the RECORD control panel.

Power line clipper transistor Q13 is used to generate a square wave from the power line sine wave fed to its base through pin 27 of plug P1. However, the square wave output from Q13 is fed to sync inverter transistor Q1 only when the SERVO REF pushbutton on the PLAY control panel is depressed for LINE reference input. When power line reference is used, the outputs of all the sync pulse generator circuits, including that of the horizontal multivibrator, will be 60-cycle pulses which are generated from the power line input.

As shown in the block diagram (figure 3), the selected reference signal is fed to the base of transistor Q1, and may be observed at test point TP1 (REF). (See figures 5A and B.) Transistor Q1 is a sync inverter amplifier which is biased so that it is normally conducting, and its collector is therefore normally clamped at −18 volts. When a negative-going signal appears at the base of Q1, the transistor is cut off and its collector potential begins to rise toward ground. The maximum value that this potential can reach, in the positive direction, is determined by monitor sync output transistor Q7, whose base is driven directly by the signal at the collector of Q1. Transistor Q7 is

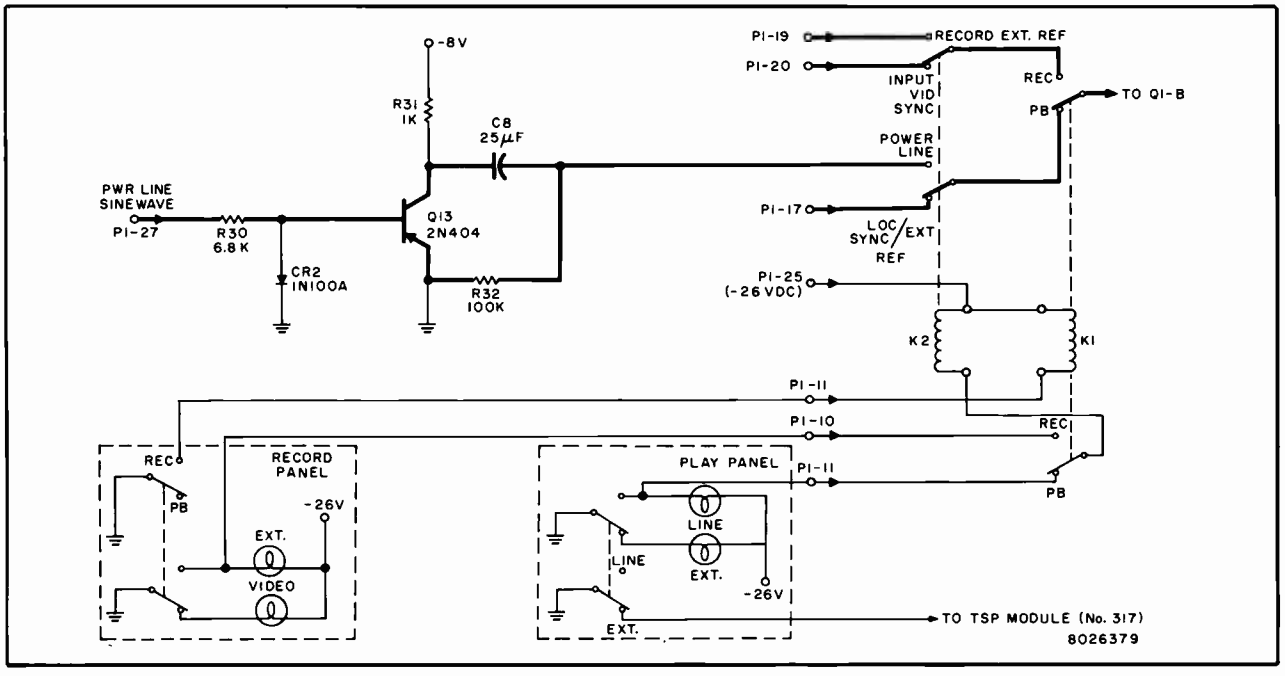
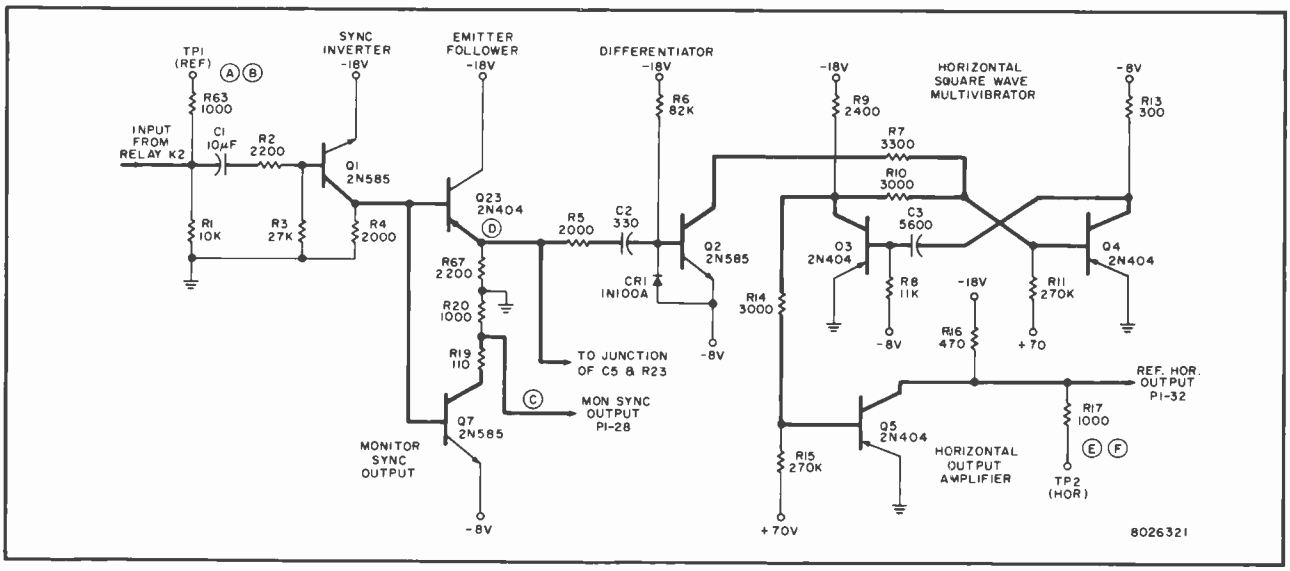
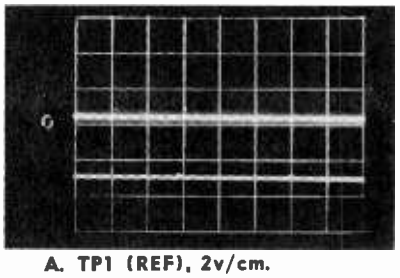
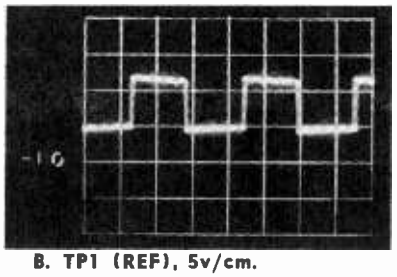


Figure 4—Power Line Clipper and Relay Circuits

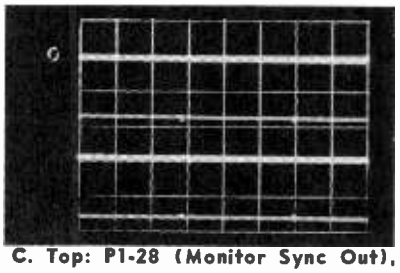




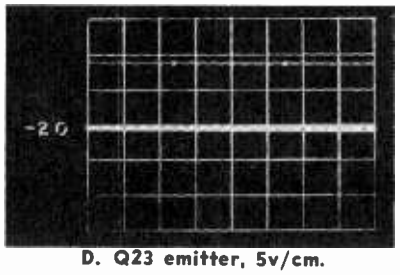
A. TP1 (REF), 2v/cm.
(EXT Servo Reference)



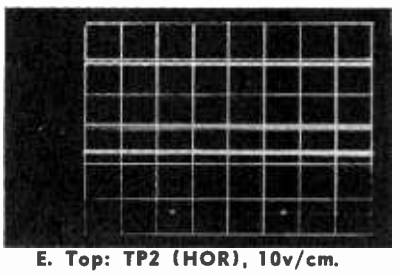
B. TP1 (REF), 5v/cm.
(LINE Servo Reference)



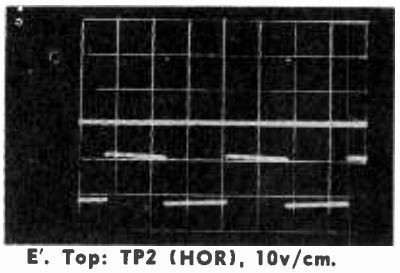
C. Top: P1-28 (Monitor Sync Out), 2v/cm.
Bottom: TP1 (REF), 2v/cm.



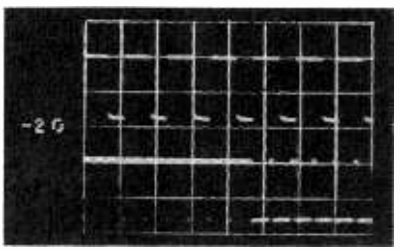
D. Q23 emitter, 5v/cm.



E. Top: TP2 (HOR), 10v/cm.
Bottom: TP1 (REF), 2v/cm.
(EXT Servo Reference)



E'. Top: TP2 (HOR), 10v/cm.
Bottom: TP1 (REF), 2v/cm.
(LINE Servo Reference)



F. Top: TP2 (HOR), 10v/cm.
Bottom: TP1 (REF), 2v/cm.
(EXT Servo Reference)
(50 μsec/cm)

Machine in STOP or STANDBY mode. All sweep times 5 msec/cm, unless otherwise noted.

Figure 5—Reference Horizontal and Monitor Sync Pulse Generator

initially biased at cut-off, and its collector is at ground potential when the collector of transistor Q1 is at −18 volts. Then, as the collector voltage of Q1 attempts to go more positive than the potential at the emitter of Q7, Q7 conducts and its collector is clamped at −8 volts. When transistor Q7 conducts, its base also clamps the collector of transistor Q1 at −8 volts. Therefore, for each negative-going pulse input appearing at the base of transistor Q1, a positive-going pulse (from −18 volts to −8 volts) appears at the collector of Q1 and a negative-going pulse (from ground to −8 volts) appears at the collector of Q7. The negative-going pulse at the collector of transistor Q7 is divided-down by the resistor combination of R19 and R20, and is fed from pin 28 of plug P1 to the CRO and picture monitors where it is terminated in 75 ohms and used as a source of external sync (figure 5C).

The positive-going pulse at the collector of transistor Q1 is also fed directly to the base of emitter follower transistor Q23, whose emitter voltage follows the voltage at the collector of Q1 (figure 5D). Transistor Q23 provides the current gain and low impedance necessary to drive transistors Q2, Q8, and Q9 in parallel. Capacitor C2 and resistor R6 form a network which differentiates the signal obtained from the emitter of transistor Q23. Differentiator amplifier Q2, normally biased at cut-off, is driven into conduction by the positive-going leading edge of the incoming sync signal applied to its base. The signal at the collector of transistor Q2 is fed to the base of transistor Q4, which combines with transistor Q3 to form the monostable horizontal square wave multivibrator.

In the multivibrator stable state, transistor Q3 is biased into conduction by the current withdrawn from its base through resistor R8 returned to −8 volts, and transistor Q4 is biased at cut-off by the combined effect of the fixed positive voltage applied to its base through resistor R11 and the ground potential at the collector of transistor Q3 when Q3 is conducting. When transistor Q2 is driven into conduction, its collector voltage drops from ground potential to −8 volts. This voltage develops a current, limited by resistor R7, which is fed to the base of transistor Q4 thus driving the transistor into conduction. While transistor Q4 is cut off, however, the potential at its collector is −8 volts and the base of transistor Q3 is at ground potential; therefore, capacitor C3 is charged to −8 volts. At the instant transistor Q4 begins to conduct, its collector voltage rises very rapidly to ground potential and the full charge across capacitor C3 is applied to the base of transistor Q3, thus cutting Q3 off.

This action begins the one-shot period of the multivibrator, and the duration of the period is determined by the discharge rate of capacitor C3 through resistor R8 toward −8 volts. The period exceeds that of half a TV line so that the multivibrator divides by two during the double rate pulses in the 9H interval of vertical blanking. Thus, the horizontal square wave multivibrator removes all vertical components and produces reference horizontal at a horizontal rate from the input reference sync signal.

Horizontal output amplifier transistor Q5 doubles the amplitude of the multivibrator output signal and isolates the multivibrator from the output load. The reference horizontal output signal is fed from pin 32 of plug P1 to the linelock module (no. 316) and may be observed at test point TP2 (HOR). (See figures 5E and F.)

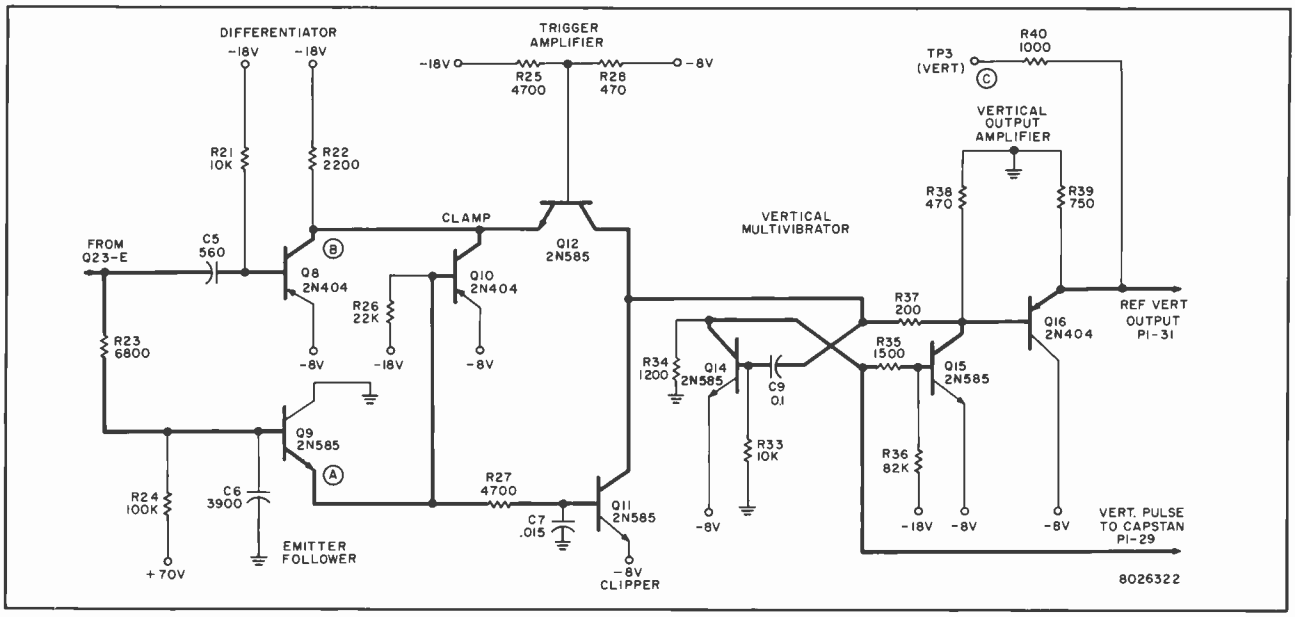
Vertical Sync Pulse Separator and Pulse Generator

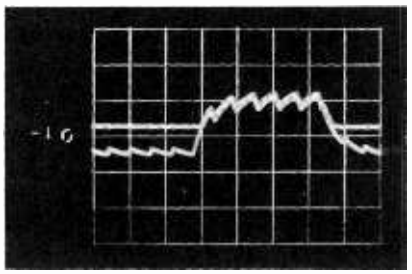
As mentioned previously, emitter follower transistor Q23 provides the current gain and low impedance necessary to drive transistors Q8 and Q9 in parallel. In the vertical sync pulse separator circuitry, the signal at the emitter of transistor Q23 is fed to the junction of capacitor C5 and resistor R23, from which it continues in two parallel paths. One of the paths is through capacitor C5 to the base of differentiator transistor Q8. The second path is through resistor R23 to the base of emitter follower transistor Q9.

Transistor Q8 functions in a manner similar to the familiar pulse narrowing boxcar circuit. The transistor is biased into conduction by the current withdrawn from its base through resistor R21 returned to −18 volts, and its collector voltage is then driven to −8 volts. When a positive-going pulse from the emitter of transistor Q23 is applied to the base of Q8 through capacitor C5, Q8 will be cut off for an interval which is proportional to the time constant determined by capacitor C5 and resistor R21.

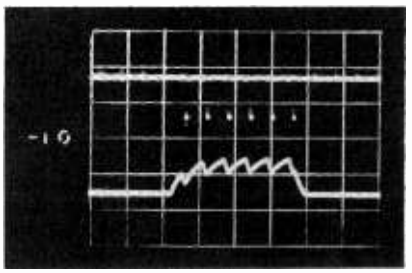
During the interval that transistor Q8 is cut off, its collector voltage attempts to fall to −18 volts. However, it is prevented from doing so because it is clamped at −8 volts by transistor Q10, which is normally saturated by the current withdrawn from its base through resistor R26 returned to −18 volts. Therefore, no signal can appear at the collector of transistor Q8 until the clamping action of transistor Q10 is removed.

Returning to the second path mentioned above, the signal from the emitter of transistor Q23 is integrated by the network consisting of resistor R23 and capacitor C6, and is then applied to the base of emitter follower transistor Q9. The time constant of the integrator network is such that the output charges to approximately 80% of its maximum amplitude within a period equal to that of one half of a TV line. Thus

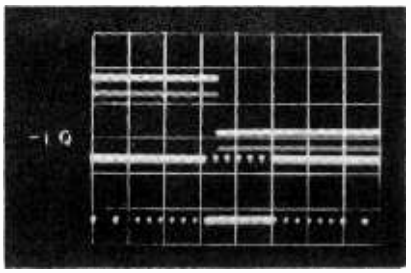




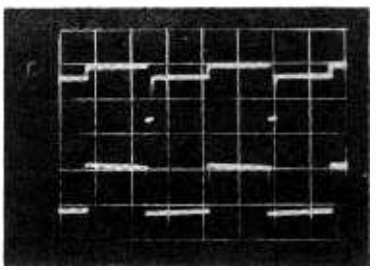
A. Top: Q9 emitter.
Bottom: Q9 base.
(50 μsec/cm)



B. Top: Q8 collector, 1v/cm.
Bottom: Q9 emitter.
(50 μsec/cm)



C. Top: TP3 (VERT).
Bottom: TP1 (REF), 2v/cm.
(EXT Servo Reference)
(100 μsec/cm)



C′. Top: TP3 (VERT).
Bottom: TP1 (REF).
(LINE Servo Reference)
(5 msec/cm)

Machine in STOP or STANDBY mode. All amplitudes 5v/cm, unless otherwise noted.

Figure 6—Vertical Sync Separator and Pulse Generator

the amplitude of the integrator network output is low when horizontal sync appears, and high when vertical sync appears.

Transistor Q9 is biased at cut-off by the voltage applied to its base through resistor R24 in conjunction with the output from transistor Q23 fed through resistor R23. When the positive-going output from the integrator network exceeds the negative cut-off bias voltage of transistor Q9, it causes Q9 to conduct. The integrated signal then appears at the emitter of Q9 as shown in figure 6A. In figure 6A, the waveform at the emitter of transistor Q9 has been superimposed

upon the waveform at its base so that the relationship between the cut-off bias voltage and the signal at the emitter may be seen. Note that the level of the cut-off bias voltage is sufficient to prevent any of the horizontal sync pulses from triggering Q9, while the greater amplitude pulse derived from vertical sync exceeds the bias voltage level and causes Q9 to conduct.

When transistor Q9 conducts, due to the integrated vertical sync signal at its base, it cuts off transistor Q10. This removes the clamping action on the collector of transistor Q8, allowing the signal from Q8 to pass to the emitter of trigger amplifier transistor Q12. The signal from transistor Q8 appears only during vertical sync, and the first pulse is the boxcar pulse derived from the leading edge of the second vertical sync pulse, as shown in figure 6B. Transistor Q12 operates as a common base amplifier, and its purpose is to amplify the signal from the collector of transistor Q8 without inverting it. When the negative-going pulse appears at the collector of transistor Q8, transistor Q12 is saturated and its collector clamps the potential at the junction of capacitor C9 and resistor R37 in the vertical multivibrator circuit at −9 volts. This places the full charge of capacitor C9 on the base of transistor Q14, thereby cutting Q14 off and beginning the multivibrator action. Thus the vertical multivibrator is triggered in effect by the leading edge of the second vertical sync pulse, as shown in figure 6C.

The signal at the emitter of transistor Q9 is also fed to the base of clipper transistor Q11, after being integrated by the network consisting of resistor R27 and capacitor C7. Normally, the potential at the base of Q11 is −9 volts (figure 7G) thus cutting the transistor off, and the collector of Q11 is then at ground potential since it follows the potential at the collector of transistor Q12 (figure 7F). When the integrated signal is applied to the base of transistor Q11, the base potential increases in a positive-going direction until it reaches the level which will allow Q11 to conduct, as shown in figure 7, F and G. If the machine is operating with a normal local sync input (vertical serrations present), transistor Q12 is triggered into conduction by the leading edge of the second vertical sync pulse, as explained in the paragraph above, and thus the collector of transistor Q11 is actually at −9 volts before Q11 begins to conduct. With normal sync input then, transistor Q11 has no effect in triggering multivibrator Q14-Q15 since the multivibrator has already been triggered by the leading edge of the pulse from transistor Q12. However, if the machine is operated with a non-standard local sync input, such as that used in industrial TV, serrations may not occur during the vertical sync interval, or may occur late. In this case, transistor Q11 generates the pulse which is used in triggering multivibrator Q14-Q15 (figure 7, H through L). (The time constant of the integrator network consisting of resistor R27 and capacitor C7 is such that transistor Q11 is forced to conduct slightly after transistor Q12 would normally conduct if the vertical serrations were present; thus transistor Q11 is prevented from producing a false triggering pulse.)

The base of transistor Q14 is connected to ground through resistor R33, and its potential is therefore positive with respect to the emitter potential; thus transistor Q14 is conducting in the multivibrator stable state. Simultaneously, transistor Q15 is cut off by the combined effect of the fixed negative bias voltage applied to its base through resistor R36 and the −8 volts at the collector of transistor Q14. The collectors of transistors Q11, Q12, and Q15 are at ground potential, and the base of transistor Q14 is at −8 volts, until a triggering pulse appears at the collectors of Q11 and Q12. Thus capacitor C9 charges to the base voltage of transistor Q14 during the interval between triggering pulses. When a triggering pulse occurs, the junction of capacitor C9 and resistor R37 is clamped at −8 volts and the full negative charge on C9 is applied to the base of transistor Q14, thus cutting the transistor off. Current is then supplied to the base of transistor Q15 through resistors R34 and R35 returned to ground, thereby driving Q15 into saturation. This action begins the one-shot period of the multivibrator, and the duration of the period is dependent upon the time constant determined by resistor R33 and capacitor C9.

The signal at the collector of transistor Q14 is a positive pulse, having an amplitude of approximately 8 volts and a period of 680 microseconds. This pulse is fed from pin 29 of plug P1 to the capstan error detector module (no. 321) in the capstan servo subsystem, where it is used in generating the reference frame pulse.

The signal at the collector of transistor Q15 is a negative pulse, also having an amplitude of approximately 8 volts and a period of 680 microseconds. This pulse is fed to vertical output amplifier transistor Q16, which operates as an emitter follower. Transistor Q16 provides the current gain necessary to drive the output signal, and also isolates the multivibrator from the output circuit. The output signal at the emitter of transistor Q16 is fed from pin 31 of plug P1 to the linelock module (no. 316) in the headwheel servo subsystem for reference purposes when the recorder is operated in the pixlock mode with TVA control. Test point TP3 (VERT) is provided for convenience in observing the output signal (figure 6C).

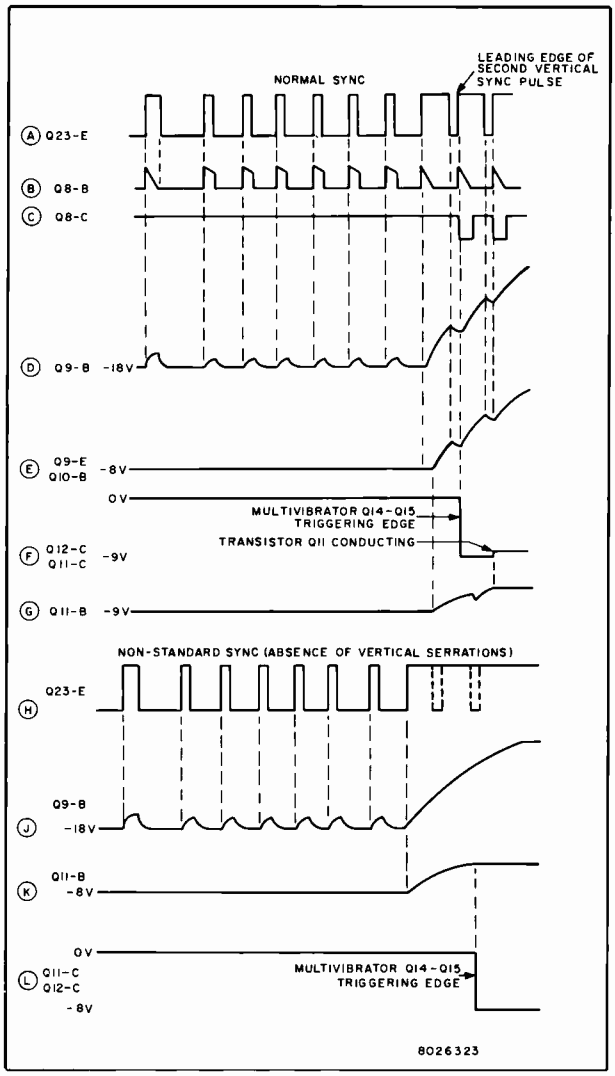


Figure 7—Waveforms Showing Development of Multivibrator Q14-Q15 Triggering Pulse

Head-Select Multivibrator and Phase Sample Pulse Generator

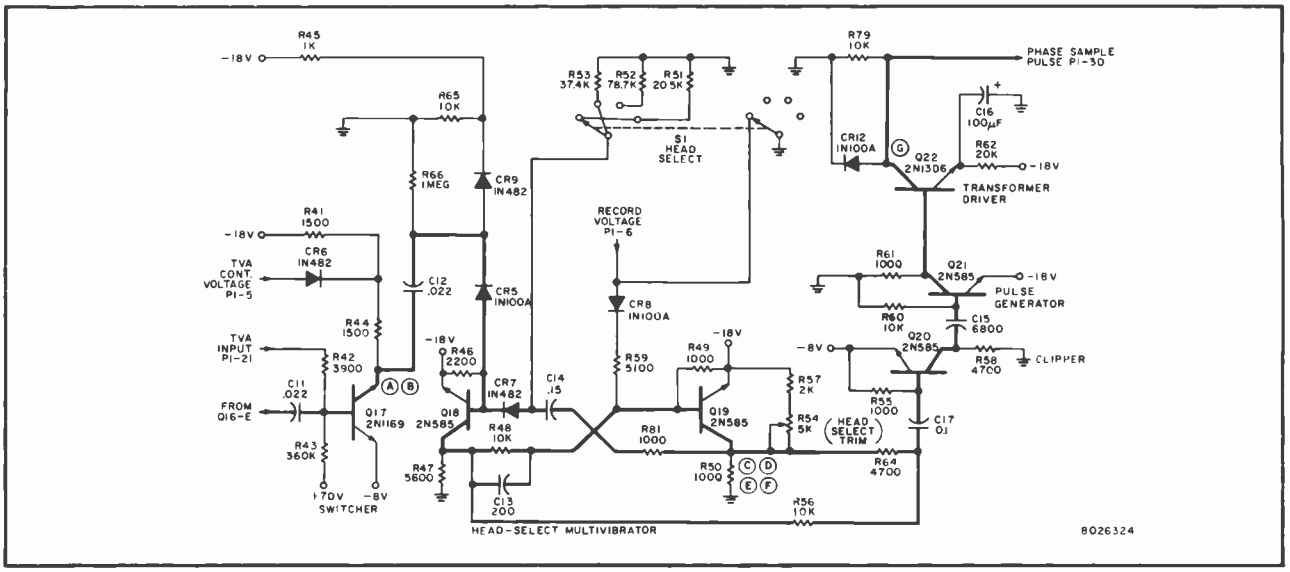
The vertical pulse at the emitter of transistor Q16 is fed through capacitor C11 to the base of switching transistor Q17. Transistor Q17 is a bidirectional junction transistor which functions as an emitter follower when the electrode connected to resistor R44 is negative with respect to the electrode connected to −8 volts, and forms part of a boxcar circuit when the relative electrode polarities are reversed.

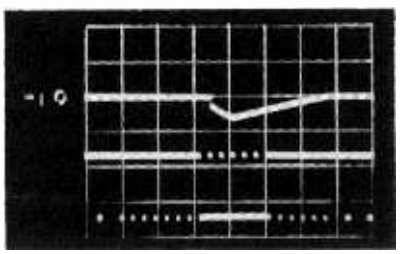
In every mode of tape recorder operation except the pixlock mode with TVA control, a control voltage of −26 volts (selected by the switch on the tape sync processor module, no. 317, in TW and SL position) is applied to the anode of diode CR6 from pin 5 of plug P1. This voltage reverse-biases CR6, thus cutting the diode off. The total resistance of resistors R41 and R44 is then in the emitter circuit of transistor Q17, and the transistor functions as an emitter follower. Capacitor C11 and resistors R42, R43 form a differentiation network which differentiates the leading edge of the vertical signal obtained from transistor Q16. The differentiated signal appears at the emitter of transistor Q17 as a negative-going pulse (figure 8A), which is then fed to the head-select multivibrator (Q18-Q19) as a triggering pulse.

When the recorder is operated in the pixlock mode with TVA control, pin 5 of plug P1 is at ground potential and diode CR6 is forced to conduct, thus connecting the junction of resistors R41 and R44 to ground. This converts the circuit of transistor Q17 into a boxcar circuit. Transistor Q17, normally conducting, is cut off by the pulse fed to its base from transistor Q16. A positive-going pulse then appears at the collector of transistor Q17 (figure 8B), and the negative-going edge of this pulse is used in triggering the head-select multivibrator. Since the positive-going pulse appears at the collector of transistor Q17 only when Q17 is cut off, capacitor C12 must charge through the path formed by diode CR9 (biased into conduction by the positive-going edge of the pulse) in conjunction with resistors R45 and R46. The values of resistors R45 and R46 are chosen so as to provide a low impedance charging path, thereby insuring an adequate rise-time of the positive-going edge of the pulse, and at the same time to prevent any additional loading effect on the negative-going or triggering edge. The negative-going edge is actually formed by the discharging of capacitor C12 through the low impedance of transistor Q17 when Q17 is saturated (during the interval between pulses fed to its base from transistor Q16).

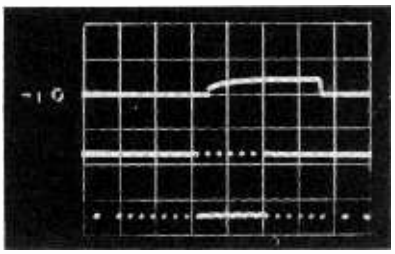
The width of the pulse at the collector of transistor Q17 is determined by the value of capacitor C11 and the control current (originating in the linelock module, no. 316) fed to resistor R42 through pin 21 of plug P1. Since the value of capacitor C11 is fixed, the pulse width is actually determined by the control current which in turn is dependent upon the error between tape and local vertical sync. Further discussion of the TVA servo loop operation appears in the headwheel servo *System* description.

Transistors Q18 and Q19 form the monostable head-select multivibrator, whose purpose is to insert any one of three different delays into the path of the phase sample pulse which is utilized by the tonewheel servo module (no. 314). The delays are provided in increments equal to the period of a quarter revolution of the headwheel, and may be selected by switching

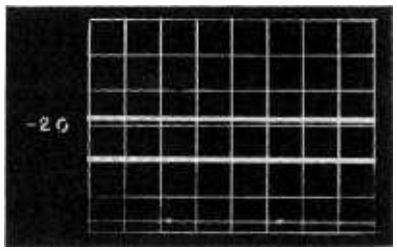




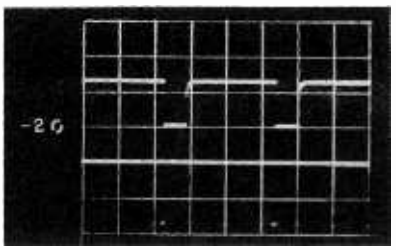
A. Top: Q17 emitter, 10v/cm.
Bottom: TP1 (REF), 2v/cm.
(Tonewheel Servo Mode)
(100 μsec/cm)



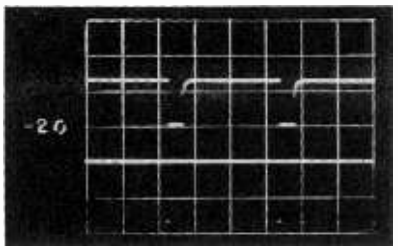
B. Top: Q17 emitter, 10v/cm.
Bottom: TP1 (REF), 2v/cm.
(Pixlock Servo Mode)
(100 μsec/cm)



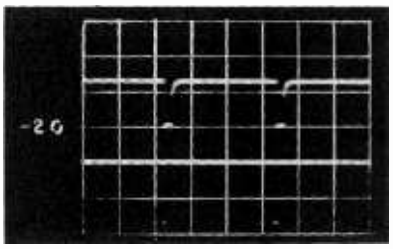
C. Top: Q19 collector, 10v/cm.
Bottom: TP1 (REF), 2v/cm.
(Head #1)



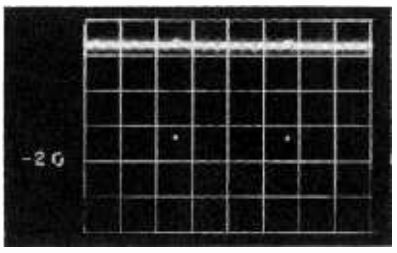
D. Top: Q19 collector, 10v/cm.
Bottom: TP1 (REF), 2v/cm.
(Head #2)



E. Top: Q19 collector, 10v/cm.
Bottom: TP1 (REF), 2v/cm.
(Head #3)



F. Top: Q19 collector, 10v/cm.
Bottom: TP1 (REF), 2v/cm.
(Head #4)



G. Q22 collector, 5v/cm.

Machine in PLAY mode. All sweep times 5 msec/cm, unless otherwise noted.

Figure 8—Head Select Multivibrator and Phase Sample Pulse Generator

the appropriate time constant network into the multivibrator circuit with switch S1 (HEAD SELECT).

Provision of the delays allows the heads to be "slipped" so that any head may play back the track containing vertical sync. In the normal tonewheel mode of operation, it is possible to "slip" heads by adjusting the capstan phasing. However, in switchlock or pixlock modes this is not possible because proper switchlock operation requires that the tracking of head and tape be maintained to insure correct alignment of the tape and local frame pulses. Therefore, with no delay introduced into the multivibrator circuit (switch S1 in position 1) capstan phasing should be adjusted so that head no. 1 is playing back vertical sync. Then, when the sample pulse is delayed with respect to the local reference pulse by an interval equal to the period of a three-quarter revolution of the headwheel, the tonewheel trapezoid (and hence head no. 1, whose position relative to the notch in the tonewheel is fixed) must follow the delay. This causes head no. 2 to play back the track containing vertical sync. Similarly, a delay equal to the period of one-half or one-quarter revolution of the headwheel will cause head no. 3 or head no. 4 respectively to play back the track containing vertical sync.

This method of "slipping" heads eliminates the need for shifting control track phasing; thus the switchlock function continues to operate normally. It should be noted that it is not possible to slip heads while the machine is playing back tape in the pixlock mode, because under these conditions the tonewheel servo does not have control of the headwheel motor. Therefore, the head desired must be selected while operating the machine in tonewheel or switchlock mode, and it is then possible to go into the pixlock mode while playing back vertical sync with the head which has been selected. However, if the HEAD SELECT switch position is changed while the machine is playing back tape in the pixlock mode and an interruption occurs which causes the servo system to automatically switch to the switchlock mode, the newly-selected head will play back vertical sync when the system "re-locks" in the pixlock mode.

Returning to the head-select multivibrator circuit, the base of transistor Q19 is connected to ground through resistor R59 and diode CR8 when switch S1 (HEAD SELECT) is in no. 1 position, thus driving the transistor to saturation. At the same time, transistor Q18 saturates due to the current supplied to its base by returning diode CR7 and resistor R51 to ground. When transistor Q17 produces an output pulse, the negative-going edge of the pulse passes through diode CR5 to the base of transistor Q18 and cuts the transistor off. This produces an output pulse at the collector of transistor Q18 which is fed through resistor R56 to the junction of resistor R64 and capacitor C17. Here the output from transistor Q18 is combined with the output at the collector of transistor Q19. Since transistor Q19 conducts continuously when switch S1 is in no. 1 position, there will be no output pulse at its collector (figure 8C); therefore, only the pulse produced by transistor Q18 will appear at the junction of resistor R64 and capacitor C17.

Placing switch S1 in no. 2 position removes the ground connection (through resistor R59 and diode CR8) from the base of transistor Q19, and transistors Q18-Q19 then function as a monostable multivibrator with a time constant determined by the values of resistors R53, R57, capacitor C14, and trimmer potentiometer R54. In the multivibrator stable state, transistor Q18 is normally saturated due to the current supplied to its base by returning diode CR7 and resistor R53 to ground, and transistor Q19 is cut off because of the negative voltage applied to its base from the collector of transistor Q18. When transistor Q17 produces a pulse, the negative-going edge of the pulse is fed through diode CR5 to the base of transistor Q18, thus cutting the transistor off. Current is then supplied to the base of transistor Q19 through resistors R47 and R48 returned to ground, and Q19 is driven into saturation. Prior to the appearance of a triggering pulse, capacitor C14 is charged to −18 volts with respect to ground. When the triggering pulse occurs, transistor Q19 saturates and the potential at the junction of capacitor C14 and diode CR7 immediately falls to −36 volts with respect to ground. Diode CR7 is reverse-biased by the negative voltage applied to its anode, so that the time constant circuit is disconnected from the base circuit of transistor Q18 during the timing cycle. Thus the leakage current of transistor Q18 and the triggering circuit is prevented from influencing the timing cycle, thereby insuring greater accuracy in timing.

With transistors Q18-Q19 operating as a monostable multivibrator, the output at the collector of transistor Q19 is a negative pulse whose positive-going edge is utilized in generating the phase sample pulse for use in the tonewheel servo module. The negative pulse at the collector of transistor Q19 is matrixed with the output from transistor Q18 through resistors R56 and R64 and, in the matrixing process, the output at the collector of Q19 always predominates (except when switch S1 is in position 1 and Q19 has no output) because of the relative collector signal amplitudes and the values of the matrix resistors. When switch S1 is in no. 2 position, the negative

pulse has a width equal to the period of a three-quarter revolution of the headwheel (figure 8D); consequently, the phase sample pulse will be delayed by the period of a three-quarter revolution of the headwheel, and the headwheel will "re-phase" to allow head no. 2 to play back the track containing vertical sync. Output pulses from the collector of transistor Q19 with switch S1 in no. 3 position (delay equal to the period of one-half revolution of the headwheel), and in no. 4 position (delay equal to the period of one-quarter revolution) are shown in figures 8E and F. Switch positions 3 and 4 then, correspond to vertical sync playback on head nos. 3 and 4 respectively.

Potentiometer R54 acts as a fine adjustment in the timing circuit to insure that each increment of delay is as nearly equal to the period of a quarter revolution of the headwheel as possible. The adjustment is made internally while observing the tape and local vertical sync pulses simultaneously on an oscilloscope, with the machine operating in switchlock mode. While switching to each position of the HEAD SELECT switch, potentiometer R54 should be adjusted so that the vertical sync pulses are aligned as closely as possible at each position of the switch (see *Adjustments*).

When the machine is operated in the RECORD mode, pin 6 of plug P1 is at ground potential and diode CR8 conducts. This connects the base of transistor Q19 to an external ground through resistor R59, and Q19 will then saturate regardless of the position of switch S1. Therefore, in the RECORD mode, no delay is introduced into the tonewheel phase reference pulse path by the multivibrator, and vertical sync will always be recorded by head no. 1.

Clipper amplifier transistor Q20, normally biased at cut-off, will conduct when the positive-going edge of the output pulse from the collector of transistor Q19 is applied to its base. The output at the collector of transistor Q20 will then be a series of negative, constant amplitude pulses which are used to drive the boxcar circuit of transistor Q21. Transistor Q21, normally conducting, is cut off by the negative pulse fed to its base. When transistor Q21 is cut off, the voltage at its collector rises toward ground potential until it reaches a level which allows transformer driver transistor Q22, normally cut off, to conduct. As transistor Q22 conducts, it clamps the collector voltage of transistor Q21 at this level for a period determined by the values of resistor R60 and capacitor C15. The level at which the collector of transistor Q21 will be clamped depends upon the bias voltage applied to the emitter of transistor Q22. This voltage in turn is determined by the repetition rate and duty cycle of the pulse output from transistor Q21, as well as by the current required by the phase sample pulse transformer in the tonewheel servo module. Diode CR12 is used to suppress the inductive kick-back of the pulse transformer.

The output at the collector of transistor Q22 is a negative-going pulse, as shown in figure 8G, and is fed from pin 30 of plug P1 to the tonewheel servo module (no. 314) as the phase sample reference pulse.

Adjustments

Normally, there are no adjustments required on the reference generator module. However, component replacement in the head select multivibrator circuit may necessitate an adjustment of potentiometer R54 in the timing circuit to insure that each increment of delay is as nearly equal to the period of a quarter revolution of the headwheel as possible. If the potentiometer must be adjusted, the following adjustment procedure may be used:

1. Place the reference generator module on a module extender, and operate the machine in PLAY mode.

2. Rotate the function selector switch on the tape sync processor module (no. 317) to SL position and make certain the switchlock function is operating correctly.

3. Rotate the HEAD SELECT switch on the module front panel to no. 1 position.

4. Press VID IN and DEMOD OUT pushbuttons on the CRO monitor switcher. Also, press the EXT SYNC pushbutton to operate the CRO monitor on external sync.

5. Adjust potentiometer R54 for a minimum displacement of tape vertical sync from head no. 1 position, while observing the superimposed waveforms on the CRO monitor.

6. Rotate the HEAD SELECT switch through each of its three remaining positions and note sync displacement. The maximum displacement at each position of the HEAD SELECT switch should be less than 50 microseconds (approximately four-fifths of a TV line).

NOTE: If the maximum displacement is exceeded at any position of the HEAD SELECT switch it will be necessary to re-adjust potentiometer R54 slightly.

REFERENCE GENERATOR MODULE (INTERNATIONAL)

Circuit Description

General

The International version of the reference generator module (no. 312) differs from the domestic version in that additional circuitry has been added to the International module to accommodate machine operation on any International line standard as well as on the domestic 525-line standard. Basically, the additional circuits accomplish the following functions: (1) cause the horizontal multivibrator to switch with line rate changes; (2) cause the vertical separator integrator time constant to vary with line rate changes; and (3) cause the head select multivibrator to switch with field rate changes.

The following paragraphs describe the operation of the circuits which accomplish the above functions; all other circuits contained in the module operate as described in the domestic reference generator module discussion. Figure 9 is the block diagram of the International reference generator module.

Horizontal Multivibrator

The purpose of the monostable horizontal multivibrator circuit in the reference generator module is to remove all vertical components from the incoming reference sync signal during tape playback or recording, and to thereby produce a reference signal occurring at a horizontal rate. The horizontal multivibrator consists of transistors Q3 and Q4, and has a one-shot period whose duration is determined by the discharge rate of capacitor C3 (figure 10). In order that the multivibrator may accomplish its purpose, its period must exceed that of half a TV line so that a divide-by-two action is attained during the double rate pulses in the 9H interval of vertical blanking.

To compensate for the difference in horizontal frequencies between the various line standards, the discharge path of capacitor C3 varies according to the line standard selected (see figure 10). When the machine is to be operated on 405-, 525-, or 625-line standards, capacitor C3 is connected to the junction of resistor R69 returned to −8 volts and resistor R70 returned to the HN bus via pin 2 of plug P1. During 405-line operation, the HN bus is at ground potential. The equivalent resistance of the base circuit time constant of transistor Q3 is then equal to the

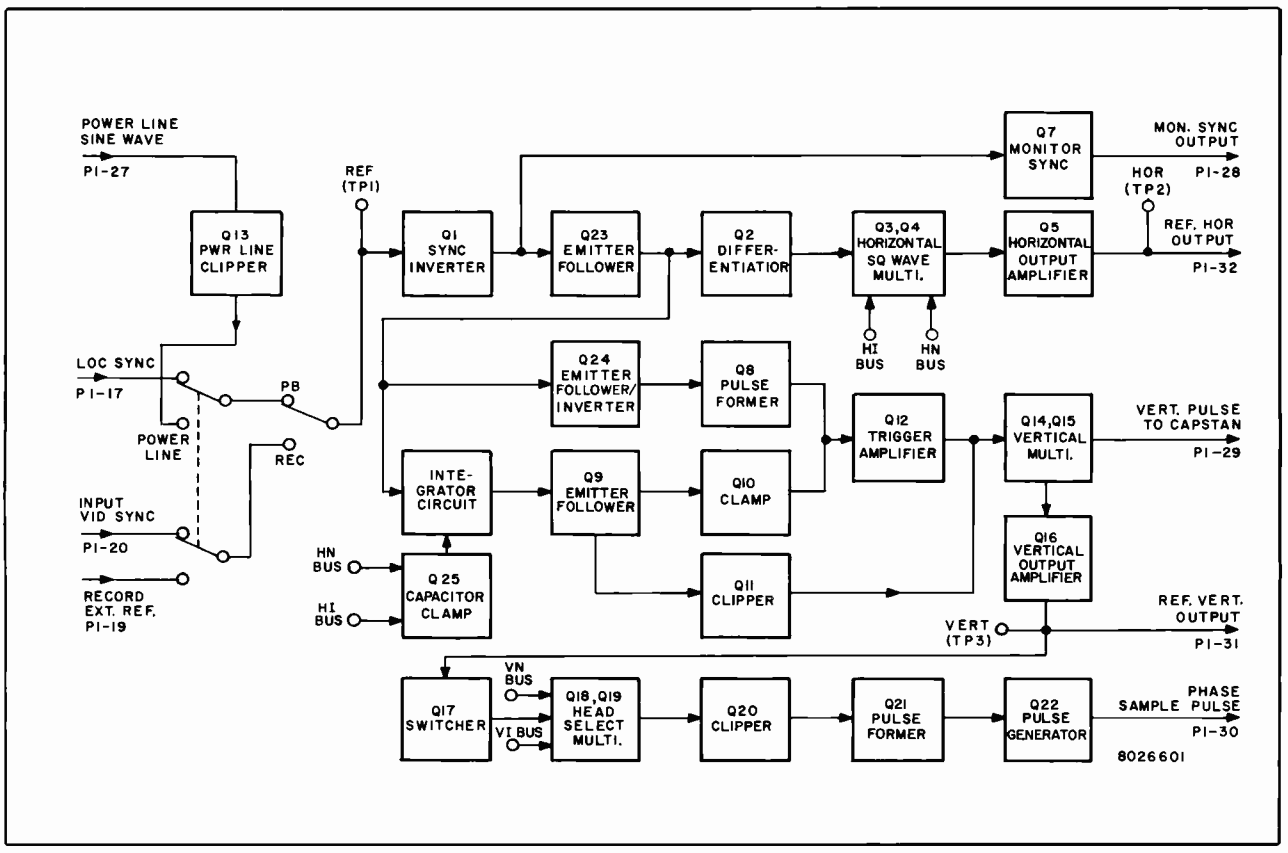


Figure 9—International Reference Generator Module Block Diagram

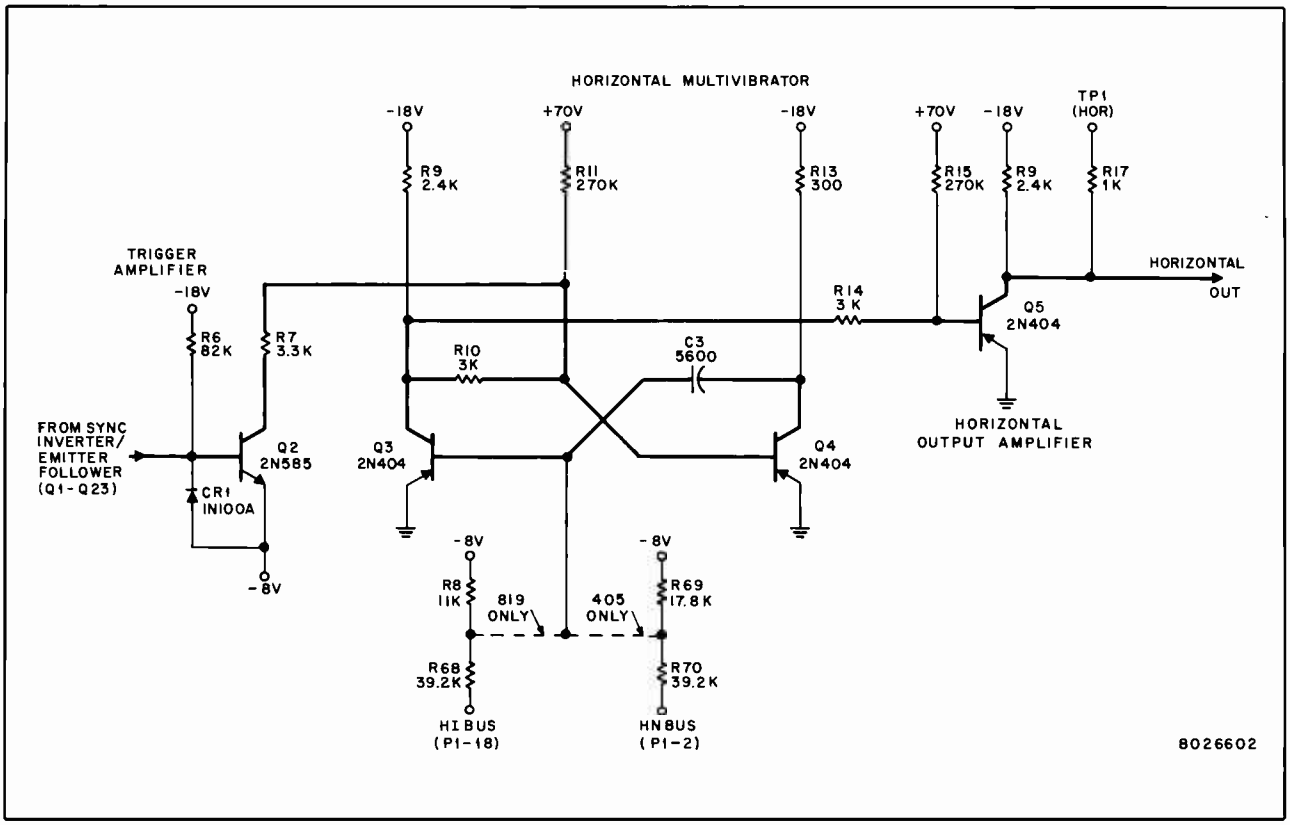


Figure 10—Horizontal Multivibrator

value of resistors R69 and R70 in parallel, and the Thevenin equivalent voltage is lower than −8 volts because of the fact that resistor R70 is returned to ground. This results in an increase in capacitor C3 discharge time, as compared with the discharge time of C3 when the machine is operated on 525- or 625-line standards and resistor R70 is returned to −20 volts via the HN bus.

When the machine is to be operated on 525-, 625-, or 819-line standards, capacitor C3 is connected to the junction of resistor R8 returned to −8 volts and resistor R68 returned to the HI bus. During 525- or 625-line operation, the HI bus is at ground potential. The equivalent resistance of the base circuit time constant of transistor Q3 is then equal to the value of resistors R8 and R68 in parallel, and the Thevenin equivalent voltage is lower than −8 volts because resistor R68 is returned to ground. In this case, the discharge time of capacitor C3 is increased during 525- or 625-line operation, as compared with 819-line operation when resistor R68 is returned to −20 volts via the HI bus.

The horizontal multivibrator time constant is thus switched in accordance with the various line standards, so that the multivibrator "on" time (unstable state) will be approximately the same percentage of a horizontal TV line regardless of the line standard used. Due to the relatively slight difference in horizontal frequency between the 525- and 625-line standards, it is unnecessary to alter the time constant when switching from one to the other of these standards.

Vertical Sync Separator

The function of the vertical sync separator circuit in the reference generator module is to utilize the incoming reference sync signal in developing a pulse during the vertical sync interval. This pulse then triggers a multivibrator at the vertical rate, and the resulting output is the reference vertical signal utilized by the headwheel servo system in obtaining phase control of the headwheel motor during machine operation in the tonewheel servo mode and in deriving the TVA control voltage when the machine is operated in the pixlock servo mode. An additional use of the tape vertical sync signal is its function in deriving the reference frame pulse in the capstan servo system.

The operation of the vertical sync separator circuit is described in detail in the domestic reference generator module discussion. Briefly, as shown in figure 11 pulse former transistor Q8, normally biased into

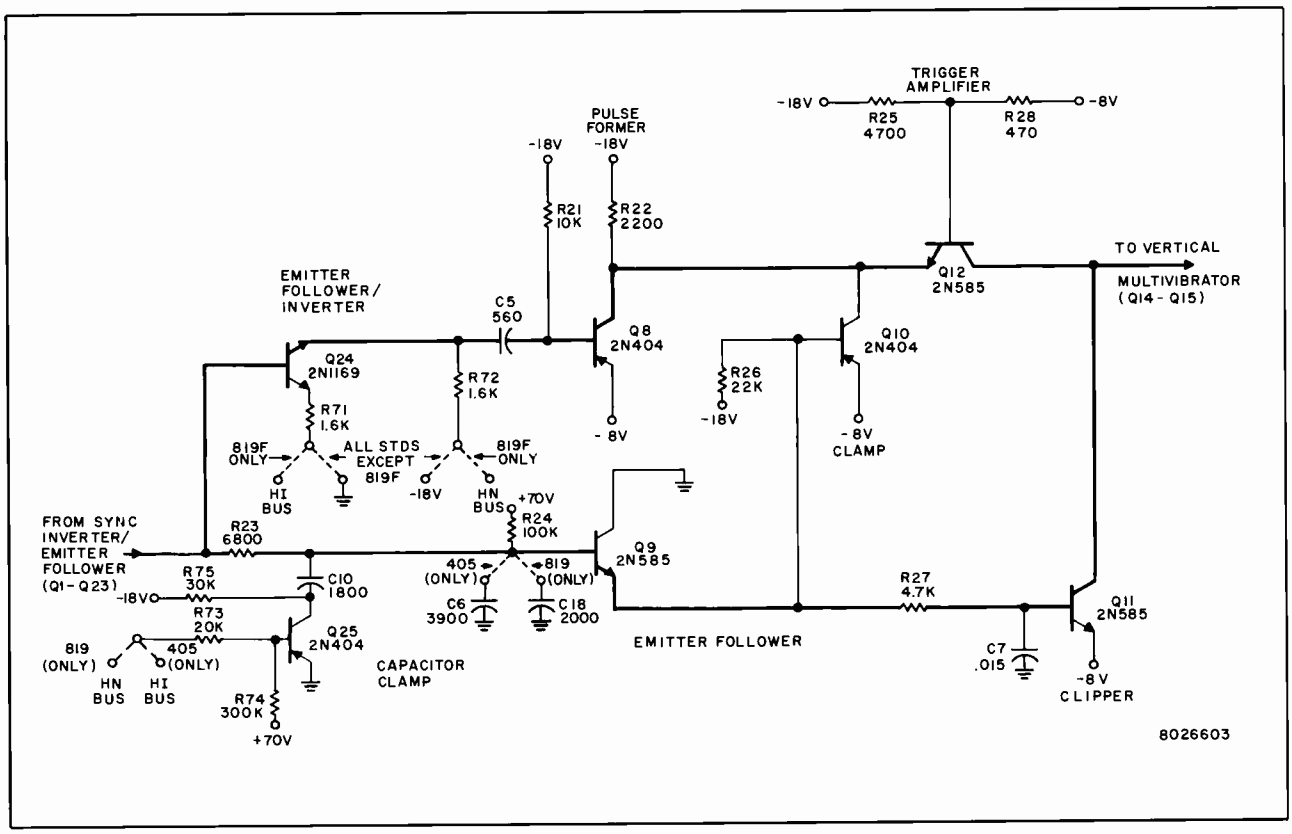


Figure 11—Vertical Sync Separator Circuit

saturation, is cut off by the positive-going portion of the signal fed to its base. When Q8 is cut off, its collector potential attempts to fall from −8 to −18 volts but is prevented from doing so by the clamping action of transistor Q10. Transistor Q10 is normally biased into saturation and its collector potential, and thus the potential at the collector of transistor Q8, will remain at −8 volts until a positive-going pulse from emitter follower transistor Q9 cuts Q10 off. The positive-going pulse appears at the base of transistor Q10 when transistor Q9, normally cut off by the biasing arrangement in its base circuit, is driven into conduction by the positive-going portion of the integrated reference sync signal fed to its base.

To obtain vertical sync separation, the time constant of the integrator network in the base circuit of transistor Q9 must be such that the integrator network output charges to approximately 80% of its maximum amplitude within a period equal to that of one-half of a TV line. Thus the amplitude of the integrator network output is too low to drive transistor Q9 into conduction when horizontal sync appears, but is sufficiently high to drive Q9 into conduction when vertical sync appears. Since the time constant of the integrator network is a function of the line rate, or horizontal frequency, the International reference generator module contains the circuitry which compensates for line rate changes.

As shown in figure 11, transistor Q25 operates as a switch which controls the function of capacitor C10 in the integrator circuit. When the machine is operated on 405-, 525-, or 625-line standards, resistor R73 in the base circuit of transistor Q25 is returned to the potential on the HI bus, and capacitor C6 is connected into the integrator circuit. During 405-line operation, the HI bus is at −20 volts and transistor Q25 is biased into saturation. This causes the collector of Q25 to be at ground potential, and capacitor C10 is then in parallel with capacitor C6. If the machine is operated on 525- or 625-line standards the HI bus is at ground potential and transistor Q25 is cut off by the positive bias potential on its base, thus effectively removing capacitor C10 from the integrator circuit. Therefore, during machine operation on 405-line standards, capacitors C10 and C6 in parallel increase the integration of sync to accommodate the wider sync pulses and the slower line rate as compared with 525-line or 625-line operation.

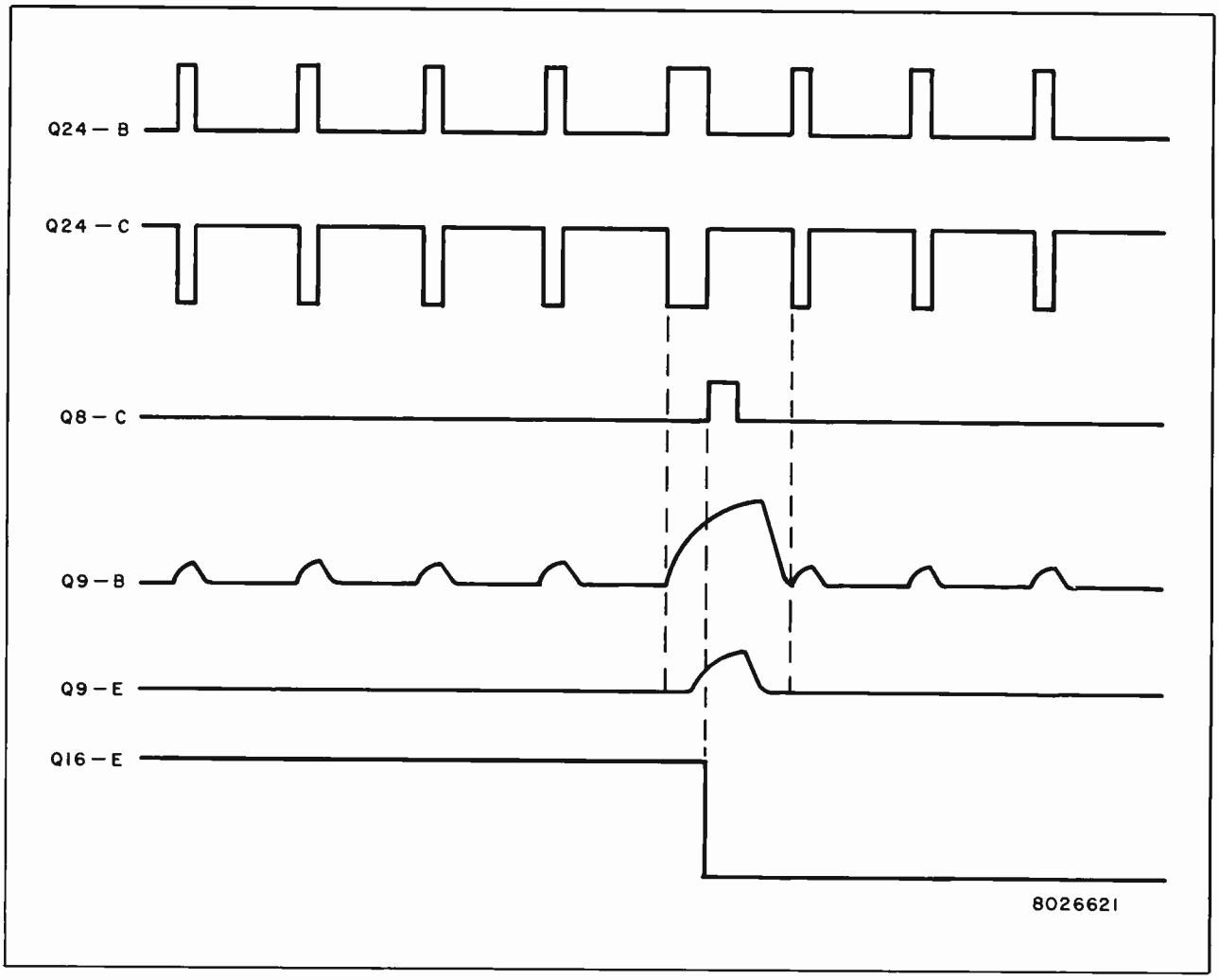


Figure 12—Vertical Sync Separation in 819-Line French System

When the machine is operated on 525-, 625-, or 819-line standards, resistor R73 in the base circuit of transistor Q25 is returned to the potential on the HN bus and capacitor C18 is connected into the integrator circuit. In this case, during machine operation on 525- or 625-line standards the HN bus is at −20 volts, transistor Q25 is saturated, and capacitor C10 is in parallel with capacitor C18. When the machine is operated on 819-line standards the HN bus is at ground potential, transistor Q25 is cut off by the positive potential at its base, and capacitor C10 is removed from the circuit. Therefore, during machine operation on 525- or 625-line standards, capacitor C10 and C18 in parallel increase the integration of sync to accommodate the wider sync pulses and slower line rate as compared with 819-line operation.

In addition to the circuit modifications noted above, the vertical sync separator circuit of the International reference generator module contains emitter follower/inverter transistor Q24. Transistor Q24 is a bilateral type; i.e., either electrode may function as emitter or collector. During machine operation on all line standards except 819-line French (819F), resistor R72 is returned to −18 volts and resistor R71 is returned to ground. The upper electrode of transistor Q24 (figure 11) then acts as the emitter and the lower electrode as the collector; thus the transistor operates as an emitter follower and the signal at its emitter appears exactly as does the signal at its base. During machine operation on 819 French standards, resistor R72 is returned to ground via the HN bus and resistor R71 is returned to −20 volts via the HI bus. This causes the upper electrode of transistor Q24 to act as the collector and the lower electrode as the emitter; thus the signal at the collector of transistor Q24 is inverted. This inversion is necessary for the separation of the single, very short, unserrated vertical sync pulse which occurs in the 819-line French system (see figure 12).

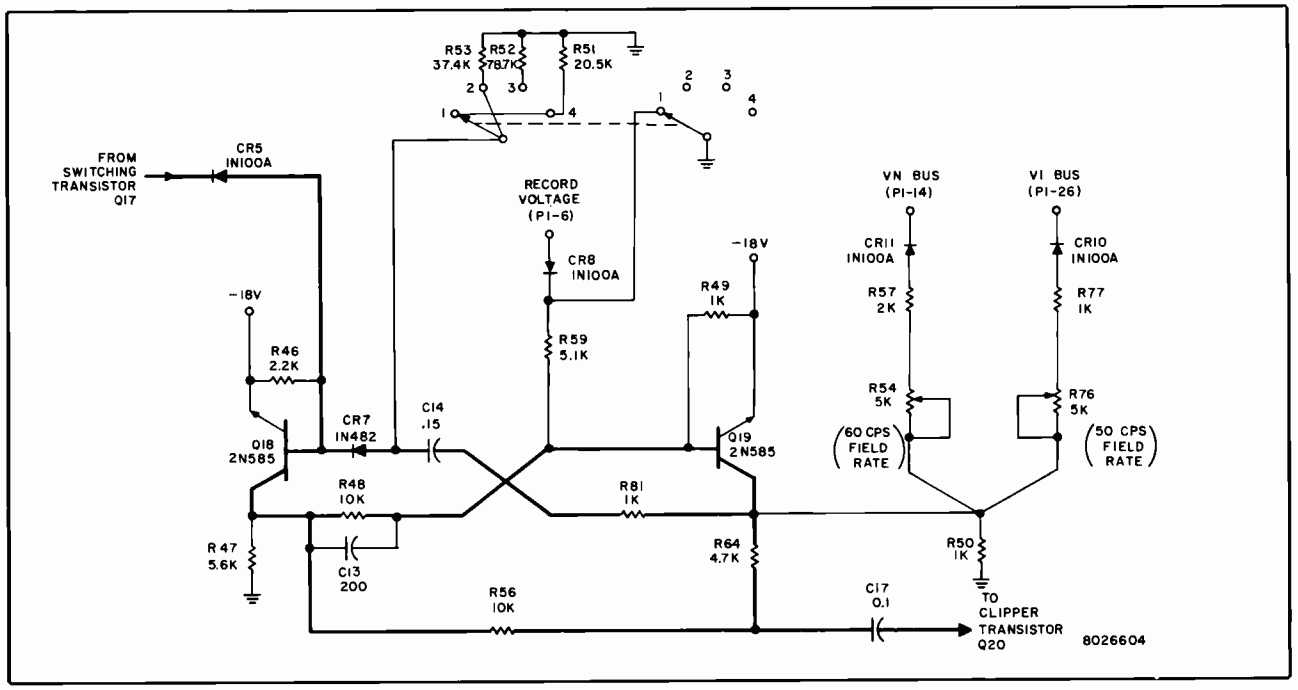


Figure 13—Head Select Multivibrator

Head Select Multivibrator

The purpose of the head select multivibrator in the reference generator module is to insert any one of three different delays into the path of the phase sample pulse which is utilized by the tonewheel servo module. The delays are provided in increments equal to the period of a quarter revolution of the headwheel, and may be selected by switching the appropriate time constant network into the multivibrator circuit with switch S1 (HEAD SELECT). A potentiometer in the head select multivibrator timing circuit of the domestic reference generator module provides a means of obtaining a fine timing adjustment so that each increment of delay may be made as nearly equal to the period of a quarter revolution of the headwheel as possible.

In the International reference generator module, two separate fine adjustment potentiometers are incorporated into the head select multivibrator circuit to accommodate machines operating with a 50-cycle field rate (250 cps headwheel rotation) or with a 60-cycle field rate (240 cps headwheel rotation). As shown in figure 13, the multivibrator timing circuit includes either head select trimmer R54, resistor R57, and diode CR11 returned to the potential on the VN bus, or head select trimmer R76, resistor R77, and diode CR10 returned to the potential on the VI bus. When the machine is operating with a 60-cycle field rate the VN bus is at −20 volts dc and the VI bus is at ground potential. Diode CR11 is then forward biased, thus placing trimmer potentiometer R54 and resistor R57 in the multivibrator timing circuit. At the same time, the ground potential on the VI bus reverse biases diode CR10 and thereby removes trimmer potentiometer R76 and resistor R77 from the timing circuit. Therefore, during 60-cycle field rate operation, potentiometer R54 is adjusted to produce essentially equal increments of a quarter revolution of the 240 cps rotation of the headwheel as the HEAD SELECT switch is rotated to each of its positions.

If the machine is operated at a 50-cycle field rate, the VI bus is at −20 volts dc and the VN bus is at ground potential. Diode CR10 is then forward biased, thus placing trimmer potentiometer R76 and resistor R77 in the head select multivibrator timing circuit. Simultaneously, diode CR11 is reverse biased, thus removing potentiometer R54 and resistor R57 from the timing circuit. During machine operation with a 50-cycle field rate then, potentiometer R76 is adjusted to produce essentially equal increments of a quarter revolution of the 250 cps rotation of the, headwheel as the HEAD SELECT switch is rotated to each of its positions. Thus the correct head select trimmer potentiometer is automatically switched into the multivibrator timing circuit according to whether the machine is operating with a 50-cycle or 60-cycle field rate.

The proper method of adjusting potentiometer R76 during 50-cycle machine operation is identical to the procedure for adjusting potentiometer R54 which is presented in the *Adjustment* section of the domestic reference generator description.

TONEWHEEL PROCESSOR MODULE

Circuit Description

General

The function of the tonewheel processor module (no. 313) is to perform five distinct processes on the tonewheel pulse which is applied directly to the module from the magnetic tonewheel (see block diagram, figure 14). The processes performed are:

1. Amplification and shaping of the tonewheel input pulse to form three separate output pulses which are fed to different locations within the machine. One of the output pulses is fed to the tonewheel servo module (no. 314) where it is used to control the velocity and phase of the headwheel motor. A second output pulse is fed to both the picture monitor and waveform monitor for display, and may also be used to synchronize the waveform monitor. (The pulse display on the picture monitor may be superimposed upon the picture by pressing the TW PULSE pushbutton on the picture monitor switcher, thus permitting a qualitative measurement of headwheel servo jitter in all headwheel servo modes.) The third output pulse is fed to the indicator module (no. 309) where it causes the headwheel (HW) indicator light above the RECORD control panel to illuminate when the headwheel is not "locked", in the tonewheel or switchlock servo mode. (This pulse is also looped through the indicator module to the FM switcher module, no. 318, for use as a control pulse in the head switching circuits.)

2. Generation of a pulse used within the module to control the "locking" of the afc loop.

3. Generation of a 4XTW output pulse, locked to the tonewheel pulse by the afc loop, which is used by the guide servo module (no. 221) for vacuum guide pressure correction.

4. Generation of a delayed 4XTW output pulse from the afc loop, used by the FM switcher module to obtain correct positioning of the 4XTW switching pulse.

5. Generation of a 2XTW motor drive sine wave, fed to the headwheel modulator module (no. 315) where it is amplitude modulated and used to drive the power amplifier, which in turn drives the headwheel motor.

An additional function of the tonewheel processor module is to provide a control voltage for the TW LOCK indicator light located above the PLAY control panel.

Pulse Amplifier and Tonewheel Multivibrator

The tonewheel pulse applied to the tonewheel processor module at pin 17 of plug P1 is developed by a change in the tonewheel magnetic head flux pattern as the notch in the tonewheel passes through the magnetic field. (The magnetic field is set up by the d-c current supplied to the magnetic tonewheel head through resistor R1 in the tonewheel processor module.) The tonewheel pulse resulting from the voltage change produced by the change in flux pattern first goes positive from the zero reference axis, maximizes, and then goes negative, crossing the zero axis to its most negative value before returning to the zero axis. Figure 15A shows the tonewheel pulse, which may be observed at test point TP1 (TW IN).

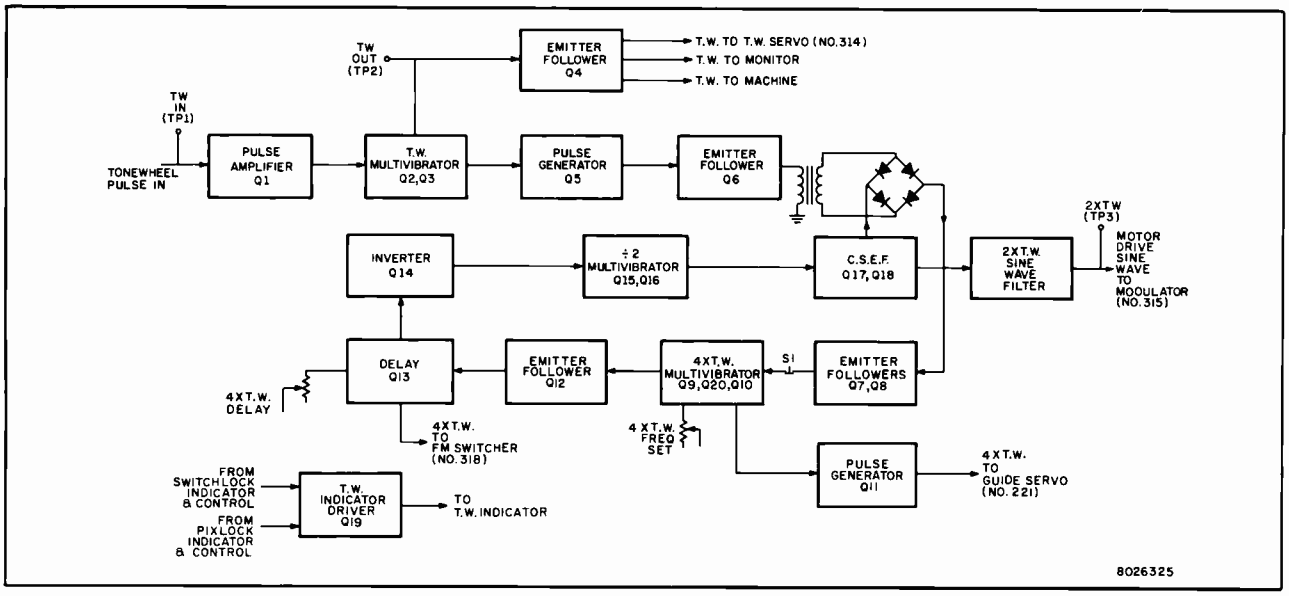
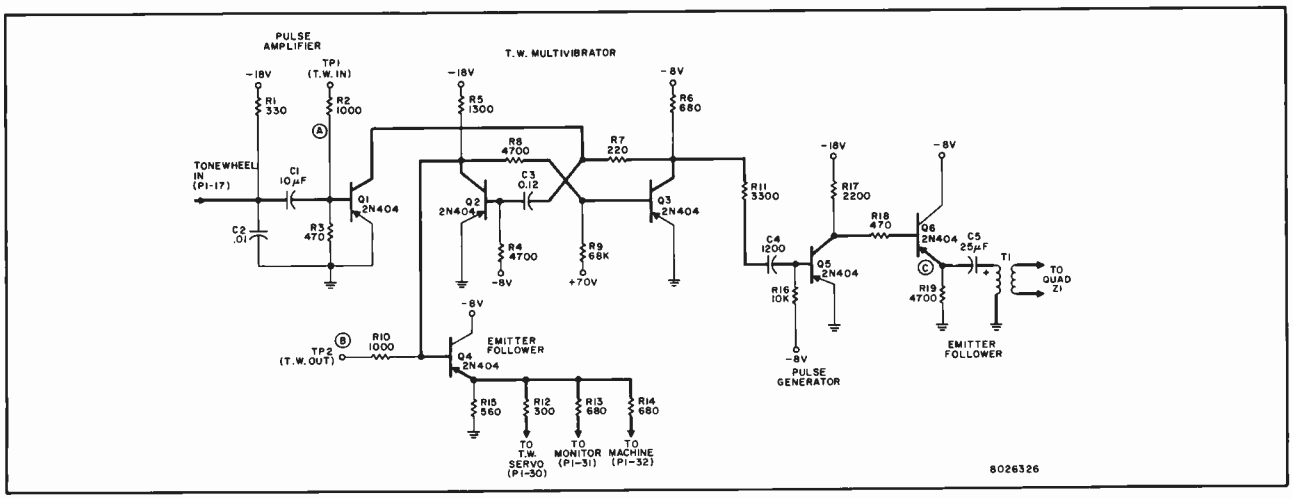


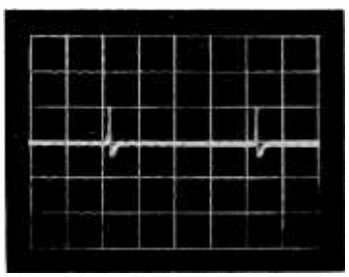
Figure 14—Tonewheel Processor Module Block Diagram

The input tonewheel pulse is applied to the base of pulse amplifier transistor Q1 which operates as a common-emitter amplifier. Transistor Q1 is normally biased at cut-off, and its collector potential is then at −8 volts. As the tonewheel pulse waveform crosses the zero reference axis in the negative-going direction, Q1 is triggered into saturation. Because of the low input impedance of transistor Q1, during saturation the negative portion of the tonewheel pulse is reduced in amplitude, as shown in figure 15A. When Q1 saturates, its collector voltage rises to approximately ground potential and a triggering pulse is thus developed. This pulse is fed to the base of transistor Q2 which combines with transistor Q3 to form a one-shot monostable multivibrator.

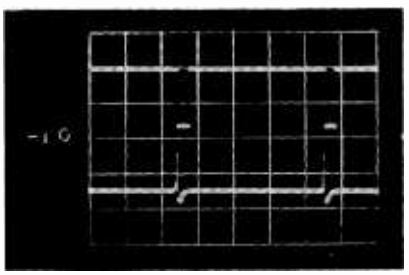
Tonewheel multivibrator Q2-Q3 is a PNP version of the NPN vertical multivibrator Q14-Q15 in the reference generator module (no. 312), and its operation is similar. The output pulse at the collector of transistor Q2 (figure 15B) is fed to the base of transistor Q4 and may be observed at test point TP2 (TW OUT). Transistor Q4 operates as an emitter follower and its purpose is to drive three separate tonewheel pulse outputs. As mentioned above in the *General* circuit description, the output tonewheel pulse destinations are the following: (1) through resistor R12 and pin 30 of plug P1 to the tonewheel servo module (no. 314); (2) through resistor R13 and pin 31 to the picture and waveform monitors; and (3) through resistor R14 and pin 32 to the indicator module (no. 309).

Since the collector currents of transistors Q1 and Q3 are common to resistor R6, the positive-going edge of the pulse at the collector of transistor Q3 corresponds to the crossover point of the tonewheel pulse (i.e., the point at which the tonewheel pulse waveform crosses the zero reference axis in the negative-going direction). The positive-going edge is then used to drive the boxcar circuit of pulse generator transistor Q5. The resultant narrow pulse output at the collector of transistor Q5 is fed to the base of emitter follower transistor Q6 which provides the current gain necessary to drive the sample pulse transformer T1 (figure 15C). The pulse output from transformer T1 forms the afc loop reference, and is used to sample the trapezoid waveform generated within the afc loop.

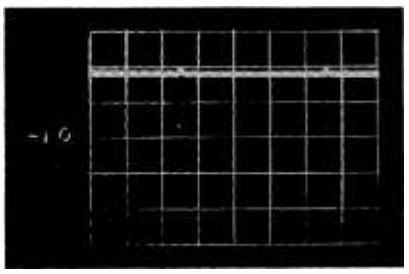




A. TP1 (TW IN), 1v/cm.



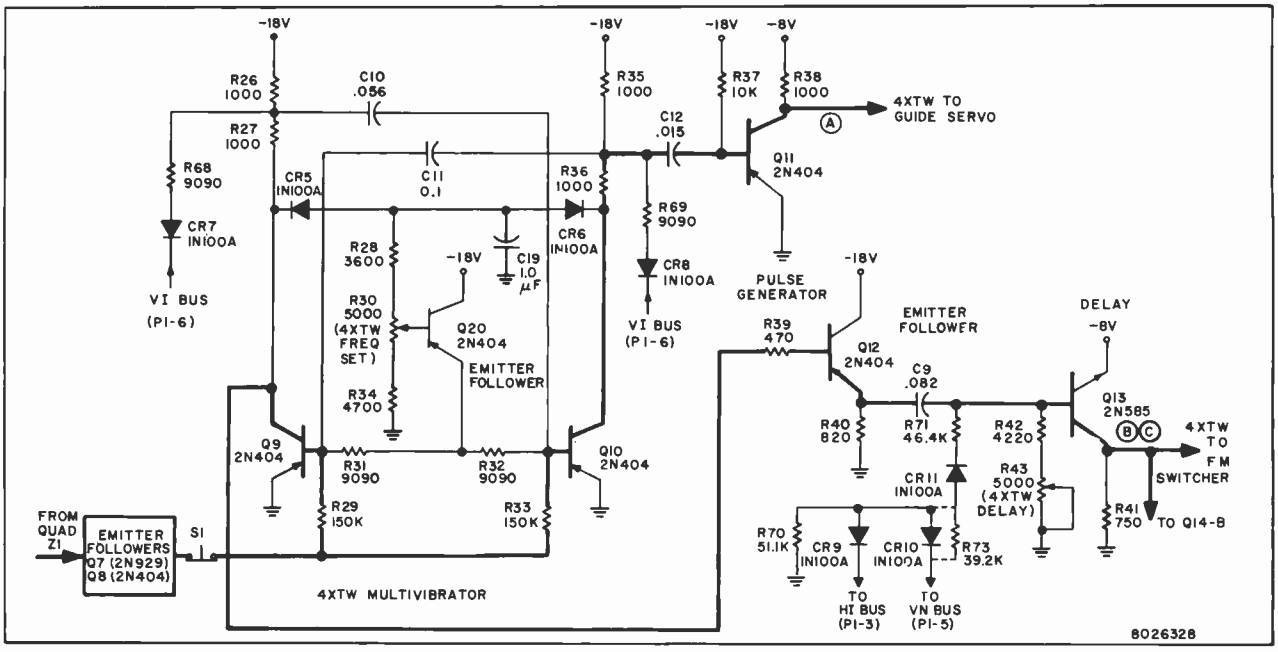
B. Top: TP2 (TW OUT), 5v/cm.
Bottom: TP1 (TW IN), 1v/cm.

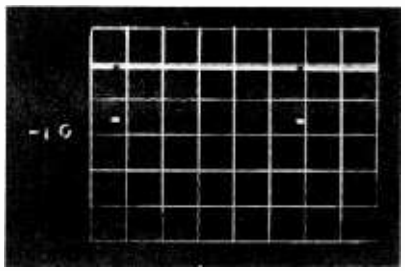


C. Q6 emitter, 5v/cm.

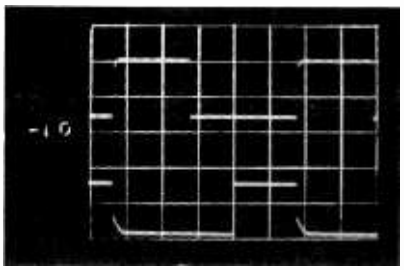
Machine in STANDBY mode. All sweep times 1 msec/cm.

Figure 15—Pulse Amplifier and Tonewheel Multivibrator

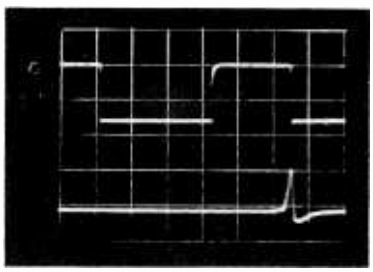




A. Q11 collector, 5v/cm.



B. Top: Q13 collector, 10v/cm.
Bottom: Q9 collector, 10v/cm.



C. Top: Q13 collector, 5v/cm.
Bottom: Q1 base, 1v/cm.

Machine in STANDBY mode. All sweep times 200 μsec/cm.

Figure 16—4XTW Multivibrator and Delay Circuits

AFC Loop

The purpose of the afc loop is to develop both the 4XTW and delayed 4XTW output pulses, as well as the 2XTW motor drive sine wave; all locked in phase to the tonewheel pulse itself. Components of the loop include the 4XTW frequency controlled oscillator, 4XTW delay generator, 4XTW divide-by-two multivibrator, trapezoid generator, sampling quad, and d-c error amplifiers.

A. 4XTW Frequency Controlled Oscillator

The 4XTW oscillator (Q9-Q20-Q10) functions as an astable multivibrator which includes a self-starting circuit and a manual frequency control circuit in addition to the automatic frequency control circuit. The following paragraphs, in conjunction with figures 16 and 17, explain the operation of the oscillator circuits:

Assume transistor Q9 to be driven into saturation and transistor Q10 to be cut off. The collector of transistor Q10 is then at −18 volts, and the base of transistor Q9 is at ground potential. This condition allows capacitor C11 to charge to −18 volts with respect to the base of transistor Q9. Then, as transistor Q10 begins to conduct, its collector voltage immediately rises to ground potential and the voltage at the junction of resistors R35 and R36 is −9 volts. Since the voltage across capacitor C11 cannot change instantaneously, the base potential of transistor Q9 is forced to +9 volts (i.e., capacitor C11 is still charged to −18 volts with respect to the base of Q9). Transistor Q9 is then cut off and its collector voltage begins falling toward −18 volts. When the collector voltage of Q9 reaches −9 volts, capacitor C10 begins to charge toward −18 volts through resistor R26 and the collector voltage then continues to follow this

slower time constant toward −18 volts. While the collector voltage of transistor Q9 is falling toward −18 volts, transistor Q10 is saturated and its base is essentially at ground potential.

Transistor Q9 will remain cut off as long as the voltage on its base remains positive. However, the positive voltage is due to the charge on capacitor C11, and this charge will leak off C11 through resistor R31 to the voltage at the emitter of emitter follower transistor Q20. Transistor Q20 conducts continuously due to the negative bias voltage applied to its base (as explained below); therefore, the voltage at its emitter is always at some negative value. Capacitor C11 will then attempt to charge to this negative value through resistor R31. At the instant the voltage on capacitor C11 goes slightly negative, transistor Q9 will be driven into conduction and C11 will be clamped at ground potential.

The charging of capacitor C11 from +9 volts toward the voltage at the emitter of transistor Q20 establishes the time interval of one half of the total multivibrator period. The second half of the period begins at the instant transistor Q9 conducts, and the sequence of operation is identical to that described above for the first half-period. The frequency of operation is inversely proportional to the sum of the two half-periods, and if potentiometer R30 (4XTW FREQ SET) is adjusted correctly (with switch S1 on the front panel pressed), the frequency of the oscillator will be exactly four times the tonewheel frequency (4XTW). (Refer to *Adjustments* for frequency adjustment procedure.)

Returning to the operation of emitter follower transistor Q20, it may be seen in figure 16 that one end of the voltage divider network comprised of resistors R28, R34 and potentiometer R30 is connected to the collector of either transistor Q9 or Q10 through diode CR5 or CR6 respectively, depending upon which diode is conducting. Forward bias is applied to the diode associated with whichever transistor is cut off and, since during normal operation only one transistor at a time is cut off, only one of the diodes will conduct at any given instant. Therefore, one end of the voltage divider is always connected to the collector of the transistor which is cut off, and the potential at that end of the divider consequently remains at approximately −18 volts. Potentiometer R30 is used to vary the negative voltage at the base of transistor Q20, thereby varying the negative emitter voltage which in turn determines the duration of one half of the multivibrator period. The purpose of emitter follower transistor Q20 then, is to isolate the loading effect of the base circuits of transistors Q9 and Q10 on the

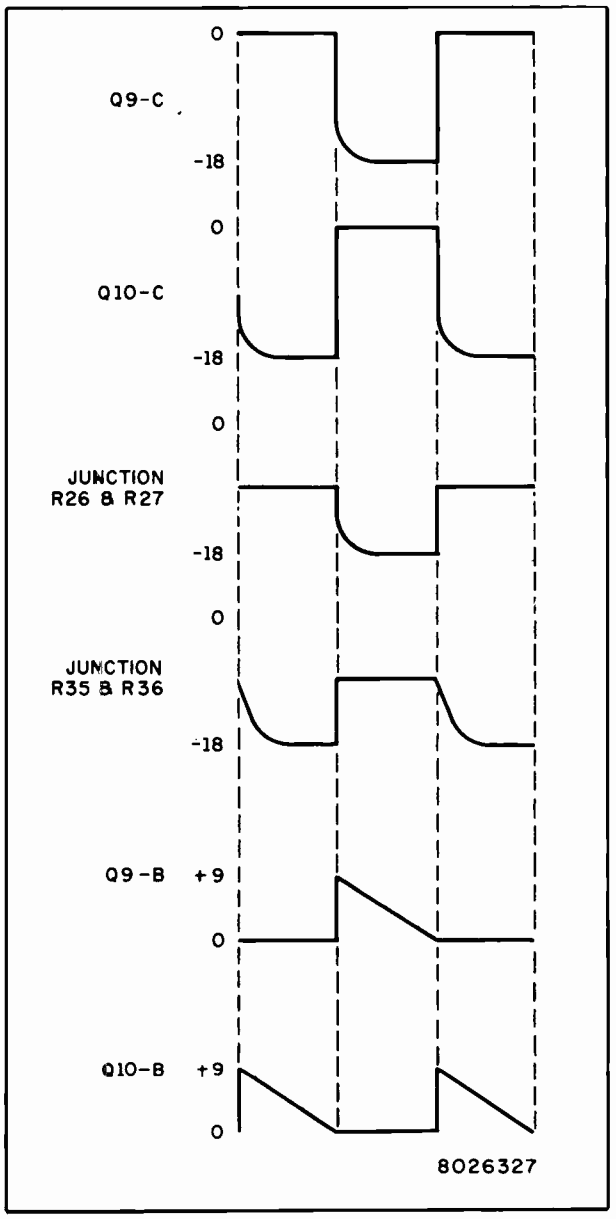


Figure 17—Oscillator Circuit Waveform Relationships

voltage divider, and to provide the base circuits with a low impedance source.

When the loop is closed, actual control of the oscillator frequency and phase with respect to that of the incoming tonewheel pulse is obtained by means of the current fed from emitter follower transistor Q8 to the base circuits of transistors Q9 and Q10 through resistors R29 and R33 respectively. This method of frequency control introduces a current into the oscillator charging circuits (C11, R31 and C10, R32) which is proportional to the tonewheel pulse frequency. The injected current either adds to or subtracts from the normal charging currents, thereby

altering the rate at which the capacitors (C11 and C10) charge toward the emitter potential of transistor Q20. As the rate of charge of each capacitor varies, the period of the multivibrator (and therefore the frequency of oscillation) changes. By utilizing this method of frequency control, any changes in the frequency of the incoming tonewheel pulse will be followed by the oscillator. (Diodes CR7 and CR8, in conjunction with resistors R68 and R69, form a network which allows a change in basic oscillator frequency when the machine is operated on International standards. For normal 525-line operation, pin 6 of plug P1 is at ground potential; thus the diodes are cut off and the network has no effect on the oscillator. In 405- or 625-line operation, diodes CR7 and CR8 are biased into conduction by −20 volts dc appearing at pin 6. This alters the voltage divider values in the multivibrator timing circuit so that the oscillator frequency is increased 4% to 1000 cycles.)

The conventional astable multivibrator (i.e., a multivibrator having base resistors connected to the supply voltage) is not inherently self-starting because both transistors may be saturated simultaneously and the circuit cannot then be regenerative. To achieve regeneration, and thus insure that multivibrator Q9-Q10 is inherently self-starting, the base resistors (R31 and R32) are connected to a supply voltage which is developed only when one or both transistors are cut off. Referring to figure 16, note that the supply voltage is developed by the circuit consisting of resistors R28 and R34, potentiometer R30, capacitor C19, transistor Q20, and diodes CR5 and CR6 connected to the collectors of transistors Q9 and Q10 respectively. From this circuit it may be seen that whenever transistors Q9 and Q10 attempt to saturate simultaneously, the voltage on base resistors R31 and R32 will be zero; therefore the base of each transistor is effectively grounded and the transistors cannot possibly saturate.

The signal at the collector of transistor Q10 is fed to the pulse narrowing boxcar circuit containing pulse generator transistor Q11. As the signal from Q10 goes in the positive direction, a narrow, negative-going pulse is produced in the collector circuit of transistor Q11 (figure 16A). This pulse is fed from pin 28 of plug P1 to the guide servo module (no. 221) where it is used in controlling the vacuum guide position.

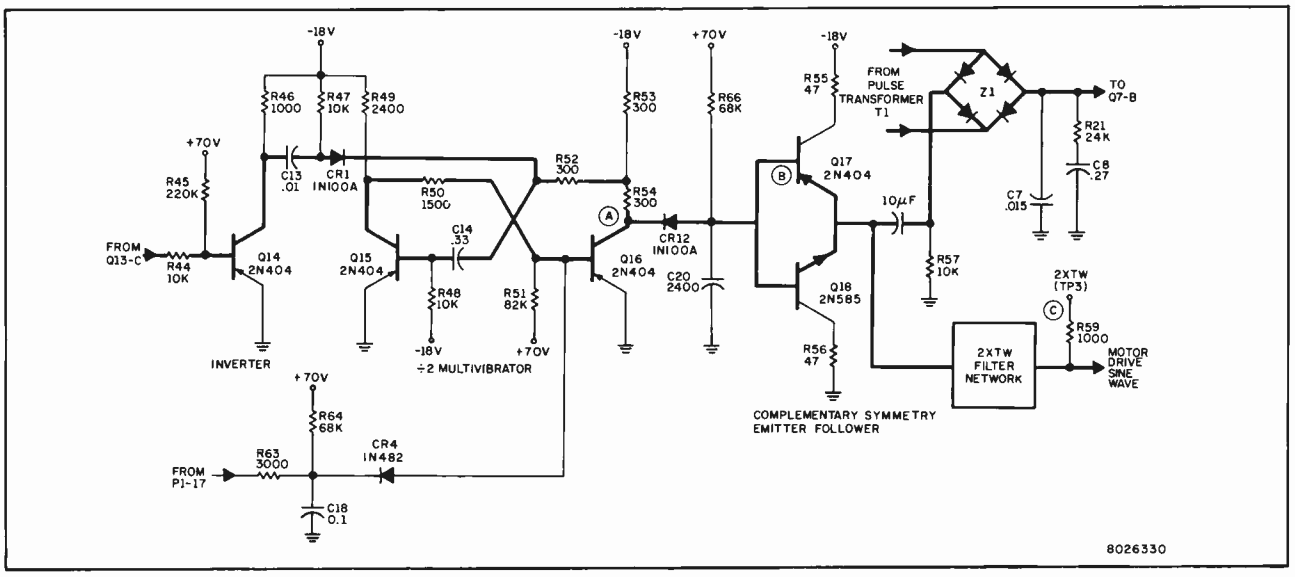
B. 4XTW Delay Generator

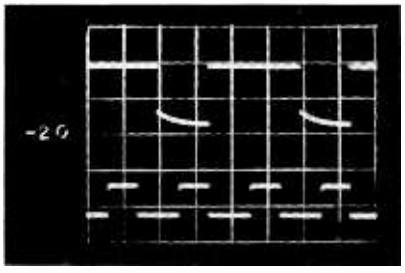
The signal at the collector of transistor Q9 (figure 16B) is fed to the base of emitter follower transistor Q12 which isolates the circuit of delay transistor Q13 from the 4XTW multivibrator Q9-Q10, and provides the current gain and low impedance necessary to drive the pulse-narrowing boxcar circuit of transistor Q13. The negative-going edge of the signal applied to the base of transistor Q13 cuts the transistor off, and a positive-going pulse appears at its collector (figure 16B). This pulse is fed from pin 29 of plug P1 to the FM switcher module (no. 318) where the positive-going leading edge of the pulse is used to insure correct switching between video heads.

Since the negative-going trailing edge of the output pulse at the collector of transistor Q13 is the edge used to generate the trapezoid waveform slope (see trapezoid generator circuit description below), this edge is locked in phase to the incoming tonewheel pulse. Therefore, by delaying the negative-going trailing edge of the output pulse, the positive-going leading edge is in effect advanced with reference to the tonewheel pulse. In addition, by making the delay variable the positive-going leading edge of the output pulse may be precisely positioned to obtain correct video head switching (figure 16C). In the afc loop, variable delay is obtained by varying the width of the output pulse from the boxcar circuit of transistor Q13. Capacitor C9, resistor R42, and potentiometer R43 (4XTW DELAY) form a network in the base circuit of transistor Q13 having a time constant which may be varied by adjusting the potentiometer. As the time constant is varied, the width of the output pulse at the collector of transistor Q13 varies so that the desired delay may be obtained. (See *Adjustments.*)

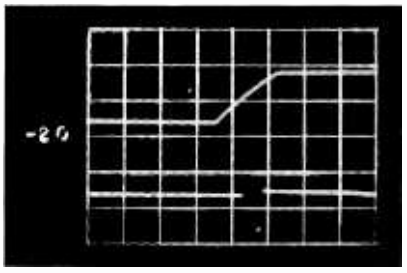
In normal 525-line operation, pin 3 of plug P1 is at ground potential, and diode CR9 is cut off. Simultaneously, pin 5 of plug P1 is at −20 volts, thereby forward-biasing diode CR10 and the diode conducts. When diode CR10 conducts, a reverse-bias voltage is applied to diode CR11. Diode CR11 is then cut off and the circuit has no effect on the time constant network. In 405-line operation, the potentials at pins 3 and 5 are reversed, but diode CR11 is again cut off and the circuit has no effect. However, in 625-line operation both pins 3 and 5 are at ground potential and diode CR11 is forward-biased. This action places resistors R70 and R71 in parallel with resistor R42 and potentiometer R43 so that the basic time constant value changes to conform to 625-line frequency operation.

NOTE: The module is normally wired for 405/525/625-line operation. If 525/625/819-line operation is required, the jumper between resistor R73 and the anode of diode CR10 must be removed and connected between the opposite end of resistor R73 and the cathode of diode CR10 (figure 16).

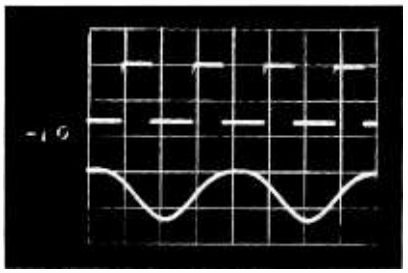




A. Top: Q16 collector.
Bottom: Q13 collector.



B. Top: Q17 base.
Bottom: Q6 emitter, 5v/cm.
(20 μsec/cm)



C. Top: Q13 collector, 5v/cm.
Bottom: TP3 (2XTW).

Machine in STANDBY mode. All sweep times 500 μsec/cm, and 10v/cm, unless otherwise noted.

Figure 18—4XTW Divide-by-Two Multivibrator and Trapezoid Generator

C. 4XTW Divide-By-Two Multivibrator

The positive-going 4XTW pulse at the collector of delay transistor Q13 is also fed to the base of inverter transistor Q14. This transistor amplifies and inverts the 4XTW pulse before it is fed to the divide-by-two multivibrator Q15-Q16. Capacitor C13 and resistor R47 form a differentiator network, and the positive-going portion of the differentiated pulse passes through diode CR1 to the base of transistor Q15 as a triggering pulse.

Transistors Q15 and Q16 form a monostable one-shot multivibrator having a period which exceeds one cycle of the 4XTW triggering pulse. The multivibrator may be triggered only when it is in its stable state; therefore, since it is in its unstable state for a period exceeding one cycle of the 4XTW triggering pulse, the multivibrator divides by two and the frequency of the signal at the collector of transistor Q16 (figure 18A) is one-half the 4XTW triggering pulse frequency (i.e., twice the frequency of the input tonewheel pulse). The operation of multivibrator Q15-Q16 is identical to that of the tonewheel multivibrator (Q2-Q3), but there is a difference in the method of triggering in that the positive-going triggering pulse applied to the base of transistor Q15 cuts the transistor off and initiates the one-shot period.

D. Trapezoid Generator

The 2XTW output pulse at the collector of transistor Q16 (figure 18A) is applied to the trapezoid generator circuit consisting of diode CR12, capacitor C20, and resistor R66. The purpose of the trapezoid generator circuit is to produce a waveform having a linear slope of specified length from the positive-going edge of the 2XTW pulse (figure 18B). Sampling on the linear slope produces a d-c output voltage which is proportional to the difference in frequency or phase between the incoming tonewheel pulse and the 4XTW pulse, and is used to correct the frequency of the 4XTW oscillator. This technique of obtaining the error voltage is known as a sampled data system.

E. Sampling Quad

The trapezoid waveform is fed to the complementary symmetry emitter follower (Q17-Q18) which provides the low source impedance and current gain necessary to drive the diode quad Z1. As mentioned above in the discussion on the pulse amplifier and tonewheel multivibrator circuits, the opposite ends of the quad are driven by the sample pulse obtained from the emitter of transistor Q6, after its phase has been split by pulse transformer T1. During the interval between sample pulses, the quad is open (cut off) and no signal current flows to the output (yellow) terminal. When the sample pulse is present, a positive pulse appears at the gray terminal of the quad, and a negative pulse appears at the red terminal. This action closes the quad, and the output voltage from the complementary symmetry emitter follower Q17-Q18 is fed directly to storage capacitor C7. The output voltage thus corresponds to the voltage on the trapezoid slope at the instant the sample pulse appears. After the sample pulse has occurred, the quad is again cut off and the charge on capacitor C7 remains until the next sample pulse occurs.

F. D-C Error Amplifiers

Emitter follower transistors Q7 and Q8 connected in cascade isolate quad Z1 from the 4XTW multivibrator circuit, and provide the current gain necessary to drive the base circuits of transistors Q9 and Q10 through resistors R29 and R33 respectively. This voltage is then fed through switch S1 to the 4XTW multivibrator (Q9-Q20-Q10), thus completing the afc loop. The gain of the loop is proportional to the slope of the generated trapezoid waveform (volts/microseconds); i.e., a short, steep slope corresponds to high loop gain, while a longer, more gradual slope corresponds to lower loop gain. Also, the afc loop gain is inversely proportional to the magnitudes of resistor R29 and capacitor C11, or resistor R33 and capacitor C10, in the 4XTW multivibrator circuit.

Although not actually a part of the afc loop, the filter network consisting of resistor R58, inductor L1, and capacitors C16, C17 utilizes the output signal from the complementary symmetry emitter follower Q17-Q18 to form the 2XTW motor drive sine wave (figure 18C). The sine wave may be observed at test point TP3 (2XTW) and is fed from pin 27 of plug P1 to the headwheel modulator module (no. 315), where it is amplitude modulated and used to drive the headwheel motor.

Fault Sensor

The network consisting of resistors R63, R64, capacitor C18, and diode CR4 (figure 18) form a protective circuit which prevents the headwheel motor from running when there is an open circuit between the tonewheel head and pin 17 of plug P1 in this module (i.e., no headwheel servo action). Protection is accomplished in the following manner:

Normally there is continuity between the tonewheel head and ground, thus placing pin 17 of plug P1 essentially at ground potential. Resistors R63 and R64 then form a voltage divider network between ground and +70 volts. This places a reverse-bias voltage on diode CR4 and the operation of multivibrator Q15-Q16 is not affected. However, if there is a discontinuity in the tonewheel head circuit, pin 17 is no longer at ground potential and resistors R1, R63, and R64 form a voltage divider network between +70 volts and −18 volts. This causes diode CR4 to receive a small amount of forward bias, thereby allowing it to conduct and provide a base drive of approximately 6 milliamperes to transistor Q16. When base drive is applied to transistor Q16, the transistor saturates and clamps the anode of diode CR4 at ground potential. Transistor Q16 will remain saturated as long as the discontinuity exists; thus the motor drive sine wave cannot be developed and the headwheel motor is prevented from running. An additional function of this circuit is to permit the machine to be operated with the headwheel panel removed.

T.W. Indicator Driver

Transistor Q19 and associated circuit components comprise the tonewheel indicator driver stage, whose purpose is to control the voltage fed to the TW LOCK indicator light above the PLAY control panel. Resistors R60, R61, and R62 form a voltage divider between −18 volts and +70 volts which provides the base of transistor Q19 with sufficient negative bias current to drive Q19 into saturation. Control voltages are also applied to the base of transistor Q19 through either diode CR2 or CR3 (from pin 20 or 4 respectively of plug P1), depending upon the recorder servo mode of operation.

The voltage on pin 20 is normally −26 volts; however, when the machine is operated in switchlock (SL) and PLAY modes simultaneously, pin 20 is grounded. This clamps the junction of resistors R60 and R61 at ground potential, and transistor Q19 will then be cut off. When transistor Q19 is cut off, the TW LOCK indicator light (connected to the collector of Q19 through pin 19 of plug P1) is turned off, and the

SW LOCK indicator light (connected to pin 20) is illuminated.

Similarly, the voltage on pin 4 is normally −26 volts; however, when the machine is operated in pix-lock (PL) and PLAY modes simultaneously, pin 4 is grounded and the junction of resistors R60 and R61 is again clamped at ground potential, thereby cutting off transistor Q19. In this instance, the TW LOCK indicator light is turned off (as is the SW LOCK indicator light) and the PIX half of the PIXLOCK indicator (connected to pin 4 of plug P1) is illuminated. (Illumination of the LOCK half of the PIX-LOCK indicator is described in the linelock module circuit description.) Resistor R62 is connected to +70 volts to insure that transistor Q19 will remain cut off when either control voltage is at ground potential.

Adjustments

Two adjustments which affect the headwheel servo operation are made at the tonewheel processor module front panel. These are the 4XTW frequency and delay adjustments. When making both adjustments, the 4XTW frequency adjustment must be made first. Test equipment required includes the *Tektronix Type 535A* oscilloscope or equivalent, and the adjustment procedure is as follows:

4XTW Frequency

1. Before attempting to adjust the 4XTW frequency, make certain that the tonewheel servo is locked to local reference with the machine in STANDBY mode (headwheel running).

2. Attach one of the oscilloscope input probes to the TW OUT test point on the tonewheel processor module.

3. Attach the second input probe to the 4XTW test point on the guide servo module (no. 221).

4. Trigger the oscilloscope from internal sync on the negative edge of the TW OUT pulse, and display exactly two tonewheel pulses in 10 centimeters.

5. Press the pushbutton on the tonewheel processor module front panel, and adjust the 4XTW FREQ SET potentiometer to obtain an exact four-to-one ratio between the signal at the 4XTW test point on the guide servo module and the signal at the TW OUT test point on the tonewheel processor. (To obtain more accurate results, use the 5X multiplier expansion for a 2% per centimeter presentation on the oscilloscope while observing the second tonewheel pulse.)

6. Release the pushbutton. The waveforms should "lock" in frequency and phase. Failure to obtain a "lock" indicates trouble within the tonewheel processor module. (To check *phase* "lock" between the waveforms, trigger the oscilloscope with external reference vertical sync. See figure 19.)

4XTW Delay

1. Make certain that the horizontal afc in the tape sync processor module (no. 317) is set up correctly, and that the 4XTW frequency is adjusted properly, before attempting to adjust the 4XTW delay.

2. Play back a test tape (machine in PLAY mode), and observe the picture monitor while varying the 4XTW DELAY potentiometer setting. When the potentiometer is rotated in one direction, white streaks will be observed entering the test pattern from one side of the picture; when the direction of potentiometer rotation is reversed, the streaks will enter the picture from the opposite side.

3. Adjust the 4XTW DELAY potentiometer to eliminate all streaks. (Make the final adjustment of the potentiometer so that it is centered in the range over which the streaks have disappeared.)

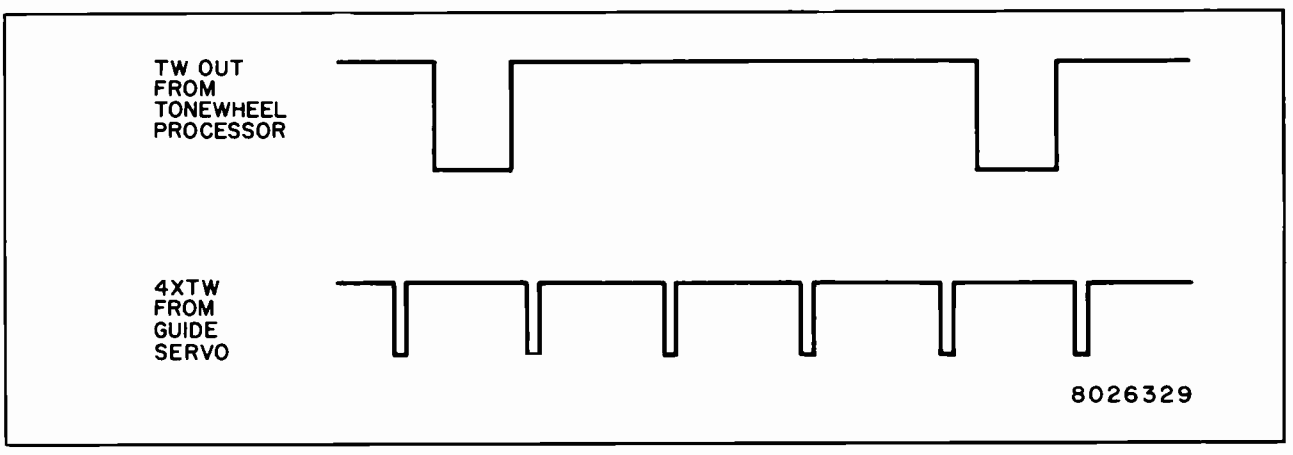


Figure 19—Waveform Relationships for Correct 4XTW Frequency Adjustment

TONEWHEEL SERVO MODULE

Circuit Description

General

In the tonewheel (or switchlock) mode of tape recorder operation, the tonewheel servo module (no. 314) controls the headwheel motor speed. Two functions are performed by the tonewheel servo module. They are: (1) the comparison of the tonewheel pulse phase to a fixed reference signal to obtain phase information for phase control of the headwheel motor; and (2) the comparison of the tonewheel pulse period to a fixed time interval. (The tonewheel pulse frequency, or reciprocal of the period, is a direct function of the headwheel motor velocity.)

The error signal generated by the tonewheel phase circuits when comparing the phase difference between the tonewheel pulses and the fixed reference signal is added to the velocity error signal generated by the tonewheel velocity circuits when comparing the difference in timing between the tonewheel pulse period and the fixed time interval. (See block diagram, figure 20.) The two error signals are combined in such a manner as to cause the velocity error signal to predominate when large errors occur, e.g. during start-up when the phase is changing rapidly. However, when the headwheel motor is running at approximately the correct speed, with only small variations in phase, the phase error signal predominates in controlling the headwheel motor speed.

The phase error signal controls the headwheel motor speed by minimizing the effect of the velocity error signal. This is accomplished by feeding a small portion of the phase error signal into the tonewheel velocity timing circuits, thereby effectively modulating the trapezoid slope so that the velocity error signal will sample at an approximately constant d-c level. This greatly reduces the effect of a change in velocity error signal, thereby allowing the change in phase error signal to exercise control of the headwheel motor. Thus the phase and velocity error signals are prevented from presenting conflicting information to the modulator module.

When the machine is switched to the pixlock mode of servo operation, prior to attaining an actual "lock" the tonewheel servo is operating in the TVA (tape vertical alignment) mode and a fixed time delay is introduced into the tonewheel pulse path. The purpose of the fixed delay is to allow the TVA servo to correct for both positive and negative errors in the location of tape vertical sync with respect to local vertical sync. Once a lock has been attained, the tonewheel error signal is disabled and the linelock error signal is enabled.

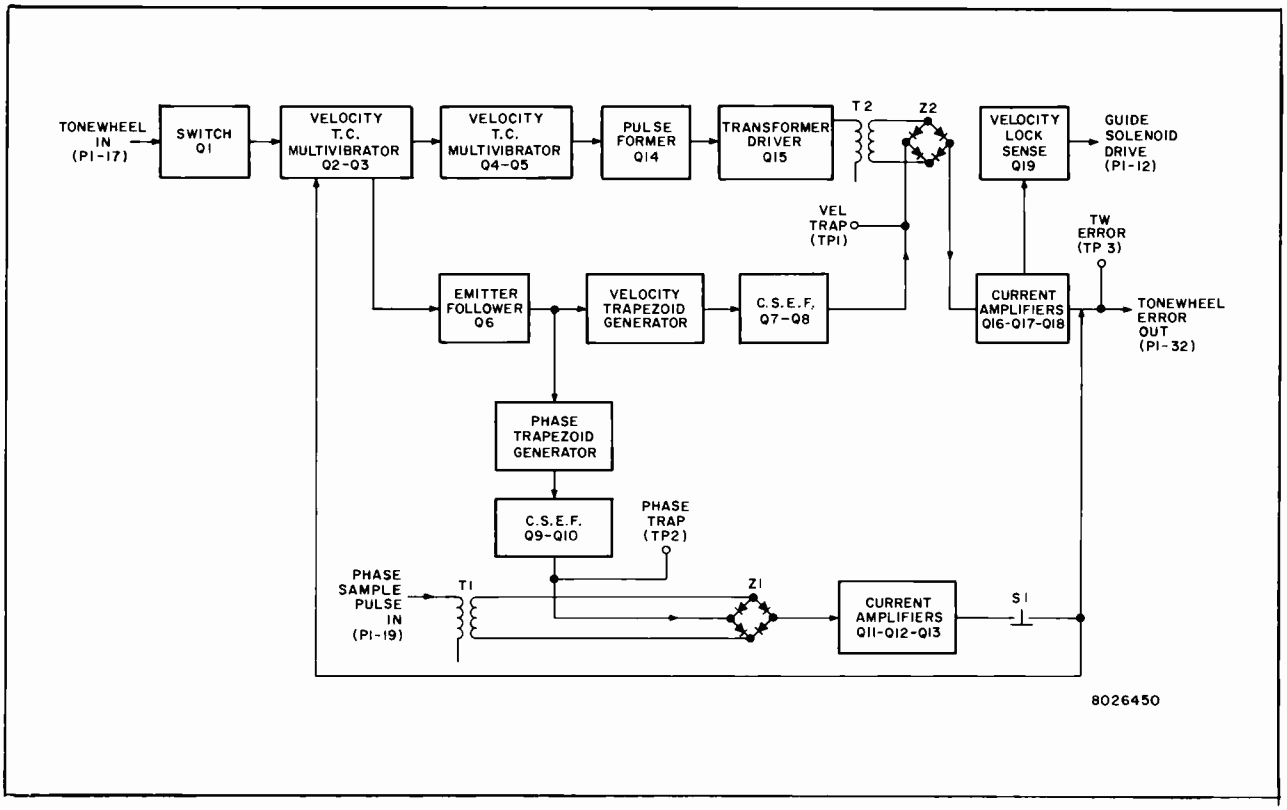


Figure 20—Tonewheel Servo Module Block Diagram

Velocity Error Detector

A. Velocity Time Constant Multivibrators

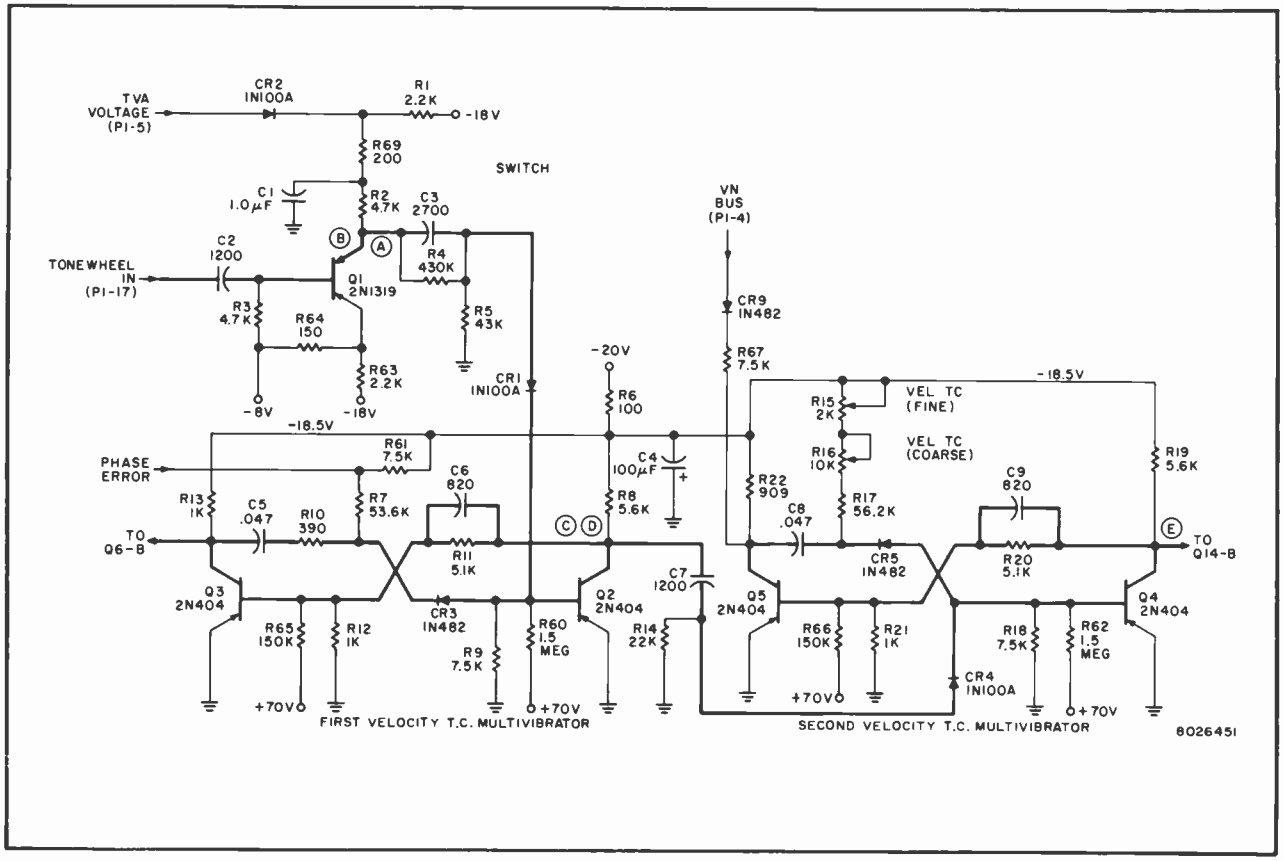
The tonewheel pulse is fed to the tonewheel servo module at pin 17 of plug P1 from the tonewheel processor module (no. 313). Capacitor C2 and resistor R3 form a differentiating network which differentiates the input tonewheel pulse before it is fed to the base of bidirectional switching transistor Q1. In tonewheel (TW) and switchlock (SL) modes of tape recorder operation, a TVA control voltage (−26 volts dc) is fed to the tonewheel servo module through pin 5 of plug P1 from the linelock module (no. 316). The control voltage reverse-biases diode CR2, and the diode is cut off. This causes the upper electrode of transistor Q1 (in figure 21) to be negative with respect to the base of Q1, and this electrode then acts as the collector of the transistor with the lower electrode acting as the emitter. Thus in the tonewheel and switchlock modes of operation, transistor Q1 is operated as a common-emitter amplifier.

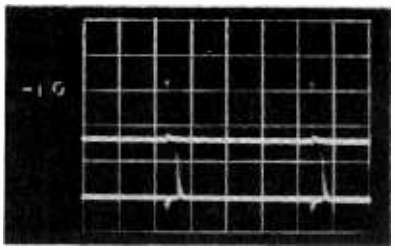
In the pixlock (PL) mode of operation, the TVA control voltage is ground and therefore the anode of diode CR2 is at ground potential. This causes diode CR2 to conduct and clamp the junction of resistors R1 and R69 at ground potential. The upper electrode of transistor Q1 is then positive with respect to the base of Q1, and this electrode acts as the emitter of the transistor with the lower electrode acting as the collector. Thus in the pixlock mode of operation, transistor Q1 is operated as an emitter follower. In any servo mode of operation then, the output signal from transistor Q1 appears at the junction of resistors R2, R4 and capacitor C3. Figure 21A shows the output signal in the tonewheel and switchlock modes, while figure 21B shows the signal in the pixlock mode. When comparing figures 21A and 21B it will be seen that in the pixlock mode the positive-going signal at the "emitter" of transistor Q1 is delayed by 360 microseconds with respect to the signal at the "collector" of Q1 in the tonewheel or switchlock mode. This is due to the fact that the tonewheel pulse from the tonewheel processor module has a multivibrator determined width of 360 microseconds, and in the tonewheel or switchlock mode switching transistor Q1 is triggered by the negative-going leading edge of the differentiated tonewheel pulse while in the pixlock mode Q1 passes the entire signal applied to its base. The fixed delay of 360 microseconds exceeds one-half of the maximum pull-in range of the TVA (tape vertical alignment) servo loop, thus enabling the servo loop to correct for both positive and negative errors of approximately 150 microseconds in the placement of tape vertical sync with respect to local vertical sync (error remaining after coarse vertical alignment by the switchlock system) when the machine is operated in the pixlock mode.

Diode CR1 passes the positive-going portion of the output signal from transistor Q1 to the base of transistor Q2 which forms a part of the monostable delay multivibrator Q2-Q3. Multivibrator Q2-Q3 is designated a velocity time constant multivibrator because its precise time constant determines approximately one-half of the fixed time interval τ (mentioned above in the *General* circuit description and shown in figure 22) which is used in determining the headwheel motor velocity. In the multivibrator stable state transistor Q2 is conducting and transistor Q3 is cut off. When a positive-going pulse appears at the base of transistor Q2 the transistor is cut off, and this in turn causes transistor Q3 to conduct. The multivibrator time constant ("off" time of transistor Q2) is determined by the charging of capacitor C5 through resistors R10, R7, and R61, and by a "velocity tickler" current injected into the timing circuit at the junction of resistors R7 and R61. (The "velocity tickler" current is a portion of the phase error signal, and is further discussed in the *Phase Error Detector* circuit description below.) When transistor Q2 is cut off, diode CR3 becomes reverse-biased due to the potential across capacitor C5. Thus diode CR1 and the base circuit of transistor Q2 are disconnected from the timing circuit during the timed period, thereby preventing any changes in transistor Q2 collector-to-base leakage current or in diode CR1 reverse current, which may be caused by temperature variations, from influencing the timing.

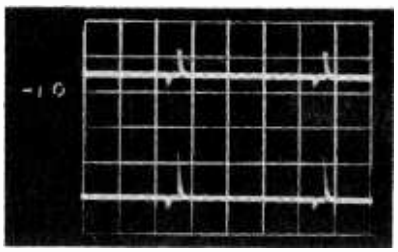
The output signal at the collector of transistor Q2 is a square wave (when the headwheel motor is running at the correct speed) having a negative-going edge timed with the positive-going triggering pulse applied to the base of Q2, and a positive-going edge corresponding to the end of the multivibrator timed period (figures 21C and 21D). This signal is fed to the base of transistor Q4 which forms a part of the second velocity time constant multivibrator Q4-Q5, and the signal at the collector of transistor Q3 is fed to the base of emitter follower transistor Q6 in the trapezoid generator circuit.

Multivibrator Q4-Q5 operates in a manner similar to that of multivibrator Q2-Q3. Transistor Q4, normally conducting, is cut off by the positive-going (delayed) edge of the signal fed to its base from the collector of transistor Q2, and this in turn causes transistor Q5 to conduct. The multivibrator time constant is determined by the charging of capacitor C8 through resistor R17 and potentiometers R15 and R16; and

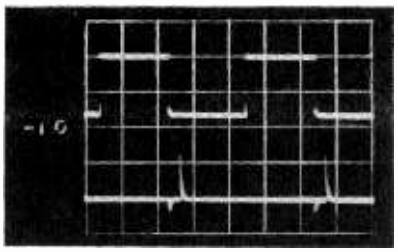




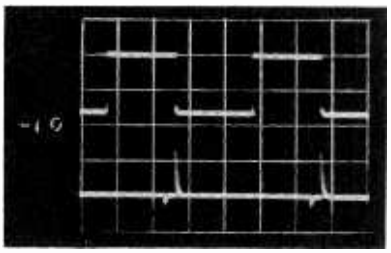
A. Top: Q1 collector.
Bottom: Q1 base.
(Tonewheel Servo Mode)



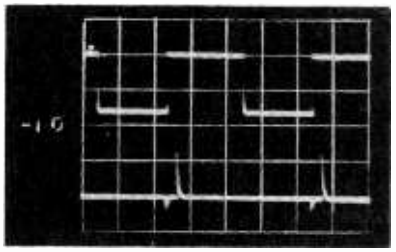
B. Top: Q1 collector.
Bottom: Q1 base.
(Pixlock Servo Mode)



C. Top: Q2 collector.
Bottom: Q1 base.
(Tonewheel Servo Mode)



D. Top: Q2 collector.
Bottom: Q1 base.
(Pixlock Servo Mode)



E. Top: Q4 collector.
Bottom: Q1 base.
(Tonewheel Servo Mode)

Machine in PLAY mode. All sweep times 1 msec/cm and amplitudes 5v/cm.

Figure 21—Velocity Time Constant Multivibrators

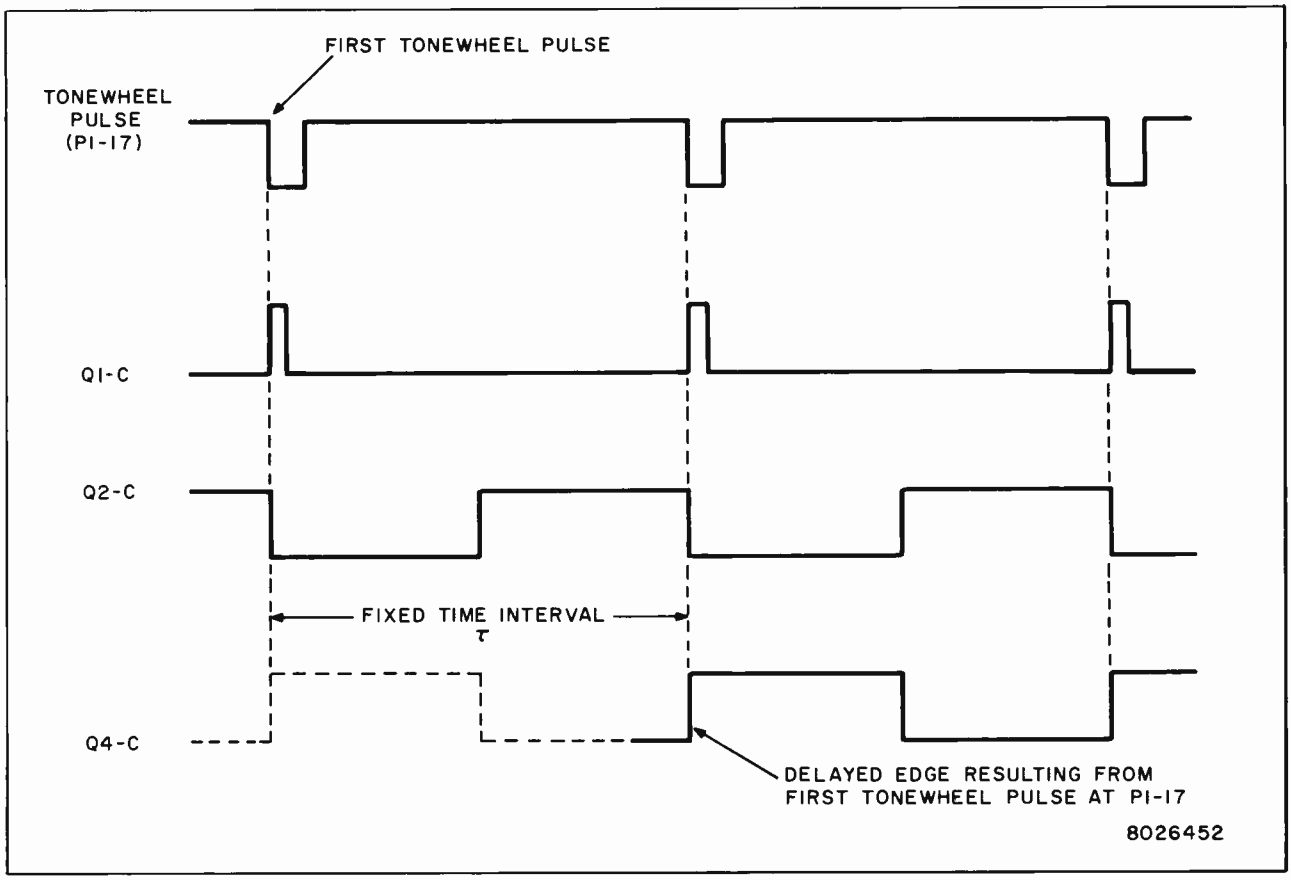


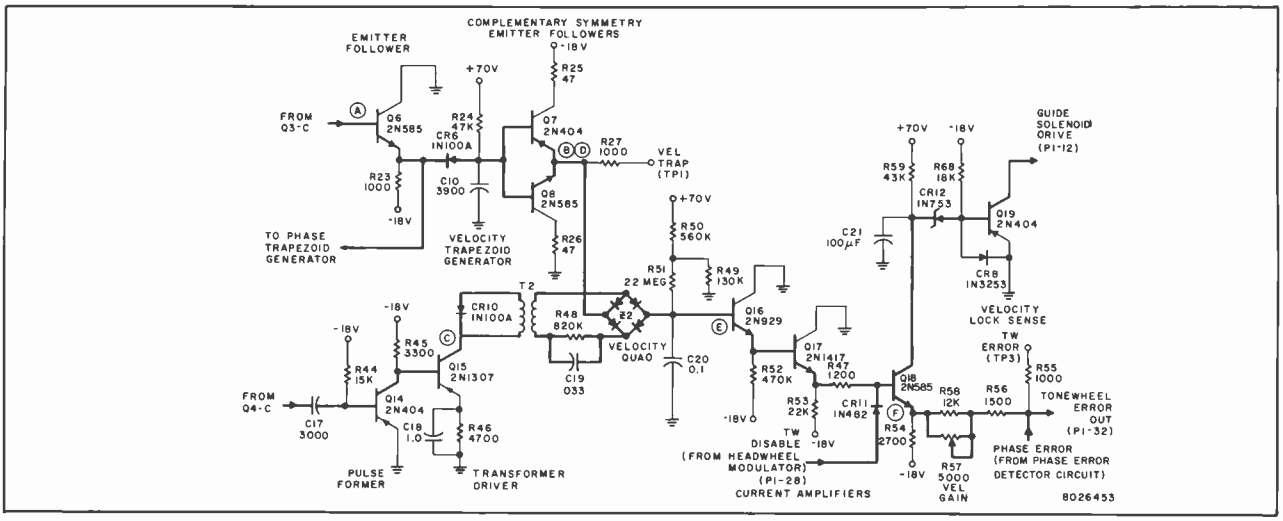
Figure 22—Waveform Timing Relationships in the Velocity Time Constant Multivibrator Circuits

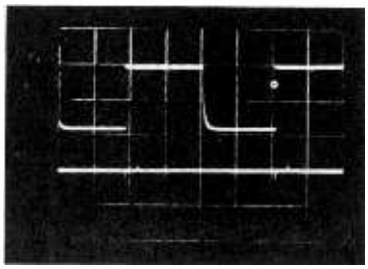
diode CR5, reverse-biased when transistor Q4 is cut off, prevents leakage currents from influencing the timing circuit during the timed interval.

The signal at the collector of transistor Q4 (figure 21E) has a negative-going edge timed to the positive-going triggering edge which is delayed by approximately one-half the fixed time interval - (figure 22) used in determining the correct headwheel velocity. Therefore, the positive-going edge of the output signal at the collector of transistor Q4 corresponds to the end of the fixed time interval τ. The net effect of both velocity time constant multivibrators then, is to produce an output signal at the collector of transistor Q4 having a positive-going edge which is delayed by one full cycle with respect to the tonewheel pulse which initiated it. Figure 22 shows the timing relationships between the input tonewheel pulse and the waveforms at the collectors of transistors Q2 and Q4 in the velocity time constant multivibrator circuits.

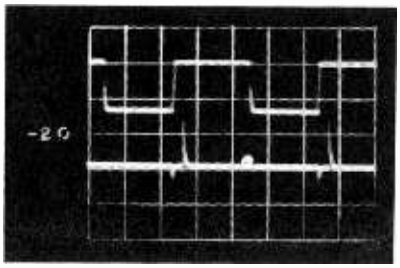
In 525-line systems the total delay (τ) provided by the multivibrators must be exactly 4166 microseconds, i.e., the period of the 240-cycle tonewheel pulse. Since the timing circuits are critical, adjustments are required to compensate for variations in component values due to tolerances, so that the exact delay may be obtained. Potentiometers R15 (VEL TC), mounted on the module front panel, and R16, mounted internally, are provided for these adjustments. The potentiometers must be set while pressing the VEL TC pushbutton (switch S1) on the module front panel so that the phase error signal will be disconnected from the timing circuit while the adjustment is made, and therefore will have no effect on the fixed time interval τ. (For actual adjustment procedures, refer to *Adjustments.*)

When operating the machine on normal 525-line standards, a bias voltage of −20 volts dc appears at pin 4 of plug P1. This voltage reverse-biases diode CR9 thus cutting the diode off, and there is no effect on the timing circuit of multivibrator Q4-Q5. However, when the machine is operated on 405- or 625-line standards pin 4 is at ground potential. Diode CR9 is then forward-biased and resistors R22 and R67 form a voltage divider network between −18 volts and ground. This reduces the time constant of the multivibrator by 4% of the total fixed time interval τ, thus allowing the tonewheel servo module to also accommodate 405-, 625-, or 819-line standards.

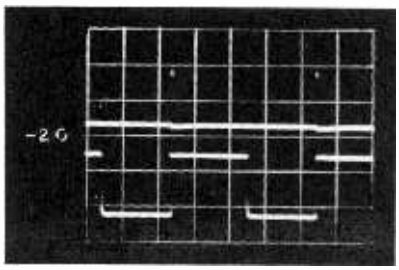




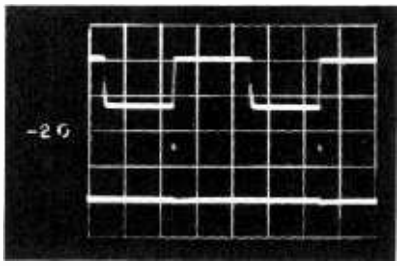
A. Top: Q3 collector, 10v/cm. Bottom: Q1 base.



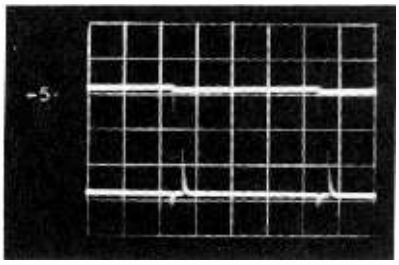
B. Top: Q7 emitter, 10v/cm. Bottom: Q1 base.



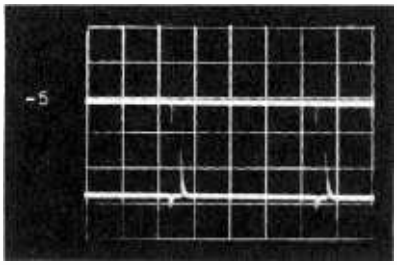
C. Top: Q15 collector, 10v/cm. Bottom: Q4 collector.



D. Top: Q7 emitter, 10v/cm. Bottom: Q15 collector, 10v/cm.



E. Top: Q16 base. Bottom: Q1 base.



F. Top: Q18 emitter. Bottom: Q1 base.

Machine in STANDBY mode. All sweep times 1 msec/cm, and amplitudes 5v/cm, unless otherwise noted.

Figure 23—Velocity Error Detector and Amplifiers

B. Velocity Trapezoid Generator

The output at the collector of transistor Q3 in the first velocity time constant multivibrator circuit (figure 23A), is fed directly to the base of emitter follower transistor Q6 whose purpose is to isolate the trapezoid generator circuit from the velocity time constant multivibrator. Transistor Q6 is driven into conduction by the positive-going edge of the signal applied to its base, and the resulting output signal at its emitter is used in generating the velocity trapezoid waveform. (The signal at the emitter of transistor Q6 is also used in generating a phase trapezoid waveform for use in the phase comparator circuit as explained below in the *Phase Error Detector* circuit description.) Diode CR6, capacitor C10, and resistor R24 form the trapezoid generator circuit, which operates in a manner similar to that of the trapezoid generator circuit in the tonewheel processor module (no. 313). The generated trapezoid waveform is fed to the complementary symmetry emitter follower transistors Q7-Q8 which provide sufficient current gain to drive velocity comparator quad Z2. The trapezoid waveform fed to the quad may be observed at test point TP1 (VEL TRAP), and is shown in figure 23B.

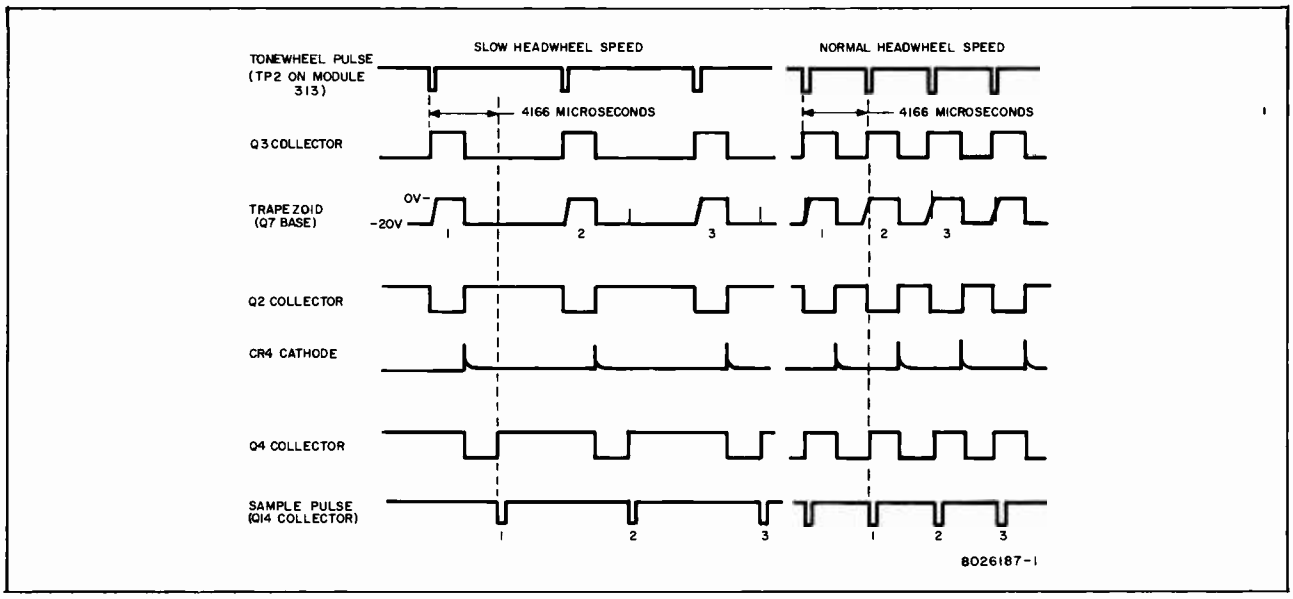


Figure 24—Waveforms Indicating Sample Pulse Positioning Relative to Reference Trapezoid Slope (525-Line Standards)

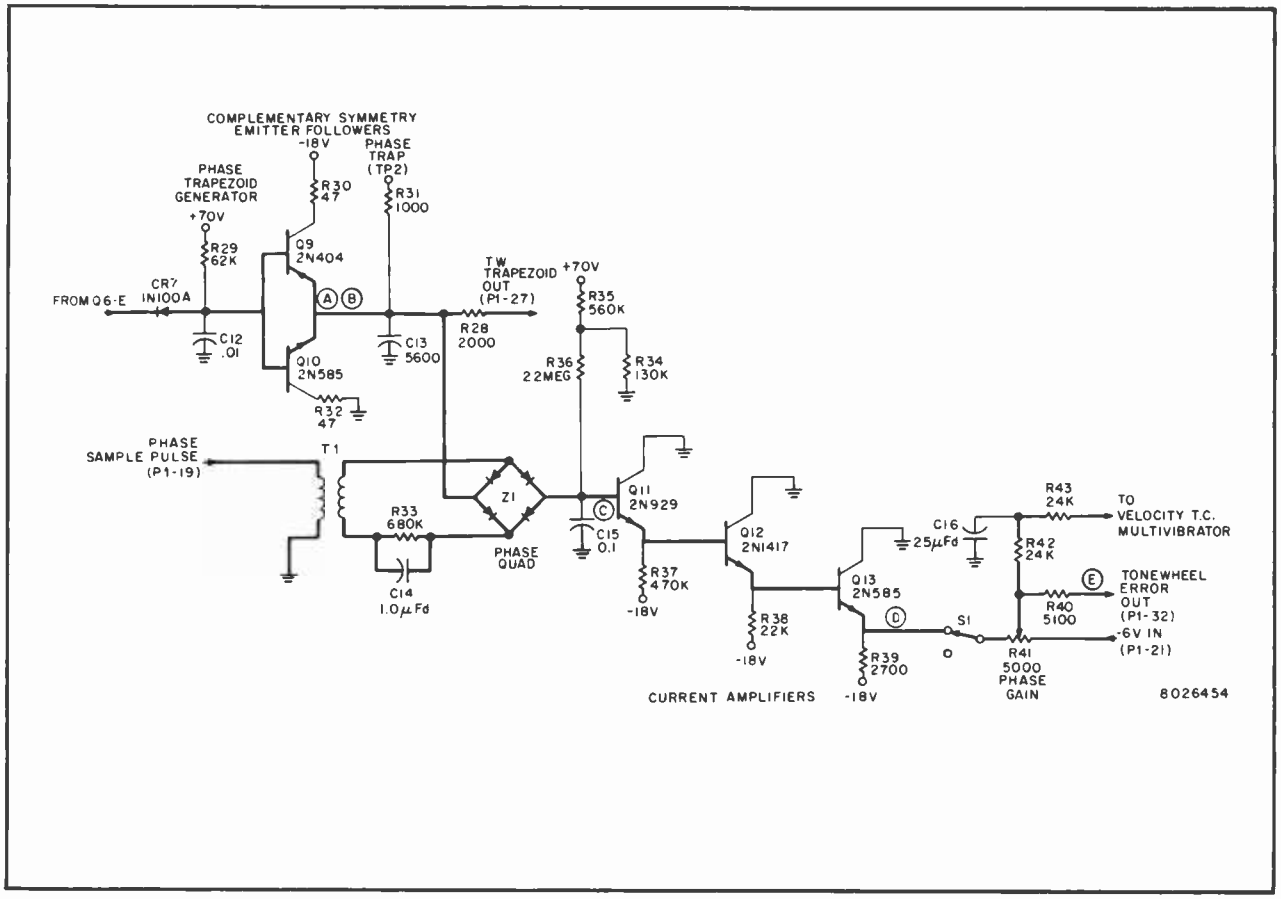
C. Velocity Sample Pulse Generator

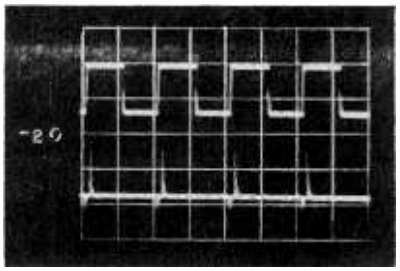
The output signal at the collector of transistor Q4 (delayed by one full tonewheel pulse cycle), is fed to the base of pulse former transistor Q14 which is a PNP version of the NPN pulse narrowing "boxcar" circuit (transistor Q21) used to generate the phase sample pulse in the reference generator module (no. 312). Transistor Q14 produces a narrow, negative-going pulse at its collector for every positive-going edge appearing at its base, and the negative-going pulse is then applied to the base of transformer driver transistor Q15. Transistor Q15 is a PNP version of the transformer driver transistor (Q22) in the reference generator module, and for every negative-going pulse applied to its base, a positive-going pulse appears at its collector (figure 23C). The positive-going pulse at the collector of transistor Q15 is fed to pulse transformer T2, and the pulse output from T2 drives the velocity comparator quad Z2.

D. Velocity Comparator Bridge Circuit and Current Amplifiers

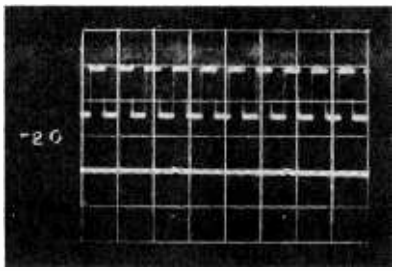
The comparator bridge circuit of velocity comparator quad Z2 operates in a manner similar to the operation of comparator quad Z1 in the tonewheel processor module, although the method by which the sample pulse drives the primary of the pulse transformer differs in each case. As explained above, comparator quad Z2 is driven by the velocity trapezoid waveform which is developed from the output waveform at the collector of transistor Q3 in the first velocity time constant multivibrator circuit, and by the velocity sample pulse developed from the waveform at the collector of transistor Q4 in the second velocity time constant multivibrator circuit (figure 23D). If the headwheel motor is running at the correct speed, the sample pulse generated by any one tonewheel pulse will sample on the slope of the trapezoid waveform generated by the following tonewheel pulse, because of the 240-cycle tonewheel pulse period delay developed by the velocity time constant multivibrators. However, if the headwheel motor is running slower than normal (as it does during start-up) the tonewheel pulses, and consequently the trapezoid waveforms, will be farther apart (figure 24). In this event, the sample pulse will occur ahead of the slope of the next trapezoid waveform, thus developing a large negative d-c error voltage which will cause the modulator to deliver full power so that maximum headwheel motor acceleration is obtained.

The d-c error voltage output from the comparator bridge circuit is fed to the base of emitter follower transistor Q16 (figure 23E). (Note that a small transient pulse occurs at the instant of sampling. This pulse is too rapid for the headwheel motor to follow, and therefore is not a significant part of the error signal.) Emitter follower transistors Q16, Q17, and Q18 in series act as current amplifiers, and the output at the emitter of transistor Q18 (figure 23F) is combined with the phase error signal through the parallel combination of potentiometer R57 and resistor R58, in series with resistor R56. (The phase error signal is obtained from the phase error detector circuit, as

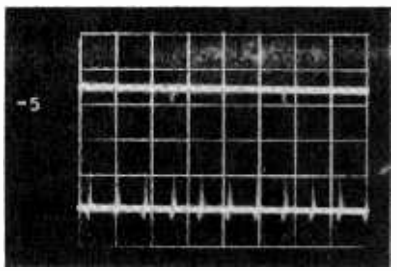




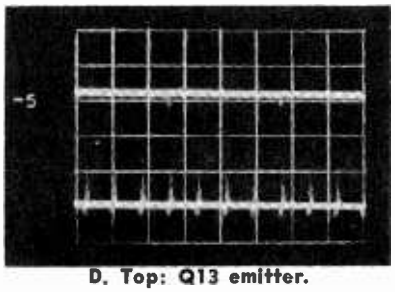
A. Top: Q9 emitter, 10v/cm. Bottom: Q1 base. (2 msec/cm)



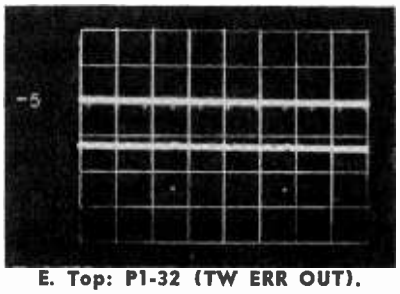
B. Top: Q9 emitter, 10v/cm. Bottom: T1 (Red), 10v/cm.



C. Top: Q11 base. Bottom: Q1 base.



D. Top: Q13 emitter. Bottom: Q1 base.



E. Top: P1-32 (TW ERR OUT). Bottom: T1 (Red), 10v/cm.

Machine in STANDBY mode. All sweep times 5 msec/cm, and amplitudes 5v/cm, unless otherwise noted.

Figure 25—Phase Error Detector and Amplifiers

explained in the *Phase Error Detector* circuit description below.) Potentiometer R57 (VEL GAIN) may be adjusted to vary the velocity error signal gain (see *Adjustments*).

Phase Error Detector

A. Phase Trapezoid Generator

The output signal at the emitter of emitter follower transistor Q6 is used in generating both the velocity and the phase trapezoid waveforms, as mentioned above. Diode CR7, resistor R29, and capacitor C12 form the phase trapezoid generator circuit which generates the trapezoid waveform in a manner similar to that of the velocity trapezoid generator circuit. (Different trapezoid waveforms are used in the phase and velocity error detector portions of the tonewheel servo to allow the loop gain of each to be optimized for its particular characteristic.) The phase trapezoid waveform is fed to complementary symmetry emitter follower transistors Q9-Q10 which provide the current gain necessary to drive the phase comparator quad Z1 (figure 25A).

B. Sample Pulse Generator

The phase sample pulse originates in the reference generator module (no. 312) where it is derived from the vertical sync of the particular servo reference being used, and thus occurs at a 60-cycle rate. In the tonewheel servo module, the sample pulse is fed through pin 19 of plug P1 to pulse transformer T1 which drives the phase comparator quad Z1. Since the phase sample pulse occurs at a 60-cycle rate, and the trapezoid waveform is generated from the tonewheel pulse occurring at a 240-cycle rate, the phase error information is obtained from every fourth trapezoid (figure 25B).

C. Phase Comparator Bridge Circuit and Current Amplifiers

Phase comparator quad Z1 operates similarly to velocity comparator quad Z2 (except that the phase sample pulse samples on the slope of every fourth trapezoid), and the d-c error voltage output from the quad is a function of the phase difference between the tonewheel pulse and the phase reference pulse derived from the particular servo reference being used. The d-c error voltage is applied to the base of emitter follower transistor Q11 (figure 25C) which operates in cascade with emitter follower transistors Q12 and Q13 to amplify the error signal current. The output from the current amplifiers (figure 25D) is fed through pushbutton switch S1, which is normally closed, to potentiometer R41 (PHASE GAIN). (Switch S1 should be open only when adjusting the velocity time constant circuit, as described under *Adjustments*.) A −6 volt dc reference voltage is also applied to potentiometer R41 (through pin 21 of plug P1), and the voltage at the center-arm of the potentiometer is then fed through matrixing resistor R40 where it is combined with the velocity error signal. The resultant error signal (figure 25E) is fed through pin 32 of plug P1 to the headwheel modulator module (no. 315) and may be observed at test point TP3 (TW ERROR).

The "velocity tickler" current mentioned above in connection with the velocity time constant multivibrator description is also obtained from the center-arm of potentiometer R41. The purpose of the "velocity tickler" current is to prevent the velocity error signal from conflicting with the phase error signal, and thereby greatly increase the phase gain when small changes in phase occur. For example, if the phase were to change slightly in a direction which would normally cause the velocity sample pulse to sample higher on the trapezoid slope, the amount of current fed into timing capacitor C5 will decrease. This in turn causes the duration of the timed period to increase slightly so that the velocity sample pulse will be returned approximately to its original position on the trapezoid slope. Resistor R42 and capacitor C16 form an integrating network whose purpose is to reduce the bandwidth of the tickler; i.e., the response is purposely made slow so that when large phase errors occur, such as during start-up when the phase error signal fluctuates rapidly as sampling occurs on different portions of the phase trapezoid waveform, the output will be small and will have little effect upon the velocity circuits. However, when the phase relationship is essentially correct, the phase error will vary slowly (at a rate which is within the integrator bandwidth) and the output amplitude will be sufficient to minimize the effect of small phase errors on the velocity circuits.

Velocity Lock Sense Control and Tonewheel Disable

The velocity lock sense control and tonewheel disable circuit (shown in figure 23) consists of transistor Q19 and associated circuit components. The purpose of this circuit is to sense the time at which the tonewheel servo has obtained a "velocity lock", and to send a command to the vacuum guide solenoid driver

when the velocity lock occurs. The vacuum guide solenoid logic circuit requires that both a velocity lock and a RECORD or PLAY command be present before the solenoid driver permits the vacuum guide to engage. For instance, in the STANDBY mode of tape recorder operation the velocity lock command is present; however, since the solenoid driver also requires a RECORD or PLAY command to cause the vacuum guide to engage, as soon as either of these commands are given the vacuum guide will engage. Therefore, there is no delay in the vacuum guide operation when switching from STANDBY to PLAY mode.

In the STOP mode there is no incoming pulse from the tonewheel processor module, thus transistor Q3 (in the first velocity time constant multivibrator circuit) is cut off and its collector is at −18 volts. Transistor Q4 (in the second velocity time constant multivibrator circuit) is then saturated, and the multivibrator cannot generate a sample pulse. Under these conditions velocity comparator bridge Z2 is "turned on" by the positive voltage obtained from the +70 volt bleeder (resistors R49 and R50) through resistor R51. The potential at the base of transistor Q16 is then essentially −16 volts (as determined by the voltage drops in the path through the bridge, the secondary of transformer T2, and emitter follower transistors Q7, Q8) and the transistor conducts, thereby applying −16 volts to the base of transistor Q17. Transistor Q17 also conducts, due to the −16 volts applied to its base, and therefore the base potential of transistor Q18 is −16 volts. However, the voltage divider network consisting of resistors R56, R54, and R58 in parallel with potentiometer R57, supplies a potential to the emitter of transistor Q18 which is positive with respect to its base potential, and Q18 is cut off. The collector of transistor Q18 is then at approximately 6.6 volts, which is equal to the sum of the contact potential of diode CR8 and the zener voltage of diode CR12.

In the initial start-up condition of the headwheel motor, sampling occurs at a d-c level of approximately −16 volts (i.e., not on the velocity trapezoid slope) and transistor Q18 remains cut off. As sampling on the trapezoid slope begins, transistor Q18 starts to conduct and the level of conduction increases as the sample pulse moves up on the trapezoid slope. The increase in conduction level of transistor Q18 causes its collector potential to fall toward −18 volts and, as the collector potential goes negative, diode CR12 is biased into conduction. Transistor Q19 is then driven into saturation by the current withdrawn from its base through transistor Q18, and by resistor R68 returned to −18 volts. The saturation of transistor Q19 is necessary to obtain one of the above mentioned commands required to trigger the vacuum guide solenoid driver.

When the machine is playing back tape in the pixlock mode, pin 28 (TW disable) of plug P1 is at ground potential, thus forward biasing diode CR11 and grounding the base of transistor Q18. This precaution is taken to insure that no disturbance in the tonewheel circuits will cut off transistor Q18 and allow the vacuum guide to become disengaged during pixlock operation. When the machine is operating in the tonewheel mode, pin 28 is at −26 volts and diode CR11 is reverse-biased, thus allowing transistor Q18 to operate normally. (The tonewheel disable control voltage fed to pin 28 of plug P1 is developed in the vertical coincidence circuit of the linelock module, and is at ground potential only when the machine is playing back tape in the pixlock servo mode.)

If the lock sense circuit detects a loss of velocity lock when the machine is operated in the tonewheel mode, transistor Q18 is again cut off. Capacitor C21 then charges toward +70 volts through resistor R59 and diode CR12 becomes reverse-biased, thus transistor Q19 remains saturated. When the voltage at the collector of transistor Q18 reaches the zener voltage of diode CR12 (due to the charging of capacitor C21 toward +70 volts), the diode breaks down and a positive voltage is applied to the base of transistor Q19. This voltage is clamped at the contact potential of diode CR8 (approximately 0.6 volt), which is sufficient to cut the transistor off. When transistor Q19 is cut off, one command to the vacuum guide driver is removed and the vacuum guide disengages.

From the above discussion and figure 23 it may be seen that the action of transistor Q18, capacitor C21, and resistor R59 is essentially that of a trapezoid generator, and that a time delay exists between the instant transistor Q18 is first cut off (loss of velocity lock) and the instant transistor Q19 is cut off. The time delay is approximately one-half second, and this prevents the vacuum guide from disengaging while the tonewheel servo recovers from any transient which causes a loss of velocity lock for less than one-half second. The time delay feature is particularly important when playing back tape in the pixlock mode, and during transitions between pixlock and tonewheel modes and vice versa.

Adjustments

The following adjustment procedures are not routine, but should be followed after initial installation of the machine and in the event faulty operation of the module requires component replacement. For routine adjustments of the velocity time constant circuit, refer to the section on systems adjustments. Test equipment required in the following procedures consists of a *Tektronix Type 535-A* oscilloscope or the equivalent.

> *CAUTION: During machine check out, observe the motor voltages on the multimeter located directly below the picture monitor. (Press HM1, HM2, and HM3 pushbuttons individually to read the motor voltages on the meter.) At start-up, the voltage for each of the three phases should be approximately 90 volts. After three seconds the voltages should decrease to approximately 35 volts to prevent the headwheel motor from "overspeeding". If the motor voltage decrease does not occur, the machine should be stopped immediately and module nos. 313, 314, and 315 should be inspected for possible faulty operation.*

Velocity Time Constant

1. Place the module on an extender, and operate the machine in the STANDBY mode.

2. Connect the input "A" oscilloscope probe to the TW OUT test point on the tonewheel processor module (no. 313), and connect the input "B" probe to the VERT test point on the reference generator module (no. 312). Display two reference vertical pulses on the oscilloscope and trigger the oscilloscope internally on the negative-going leading edge of the reference vertical pulse.

3. Adjust the oscilloscope variable sweep control so that the two reference vertical pulses are spread across exactly 10 centimeters on the oscilloscope graticule; expand the sweep using the 5X multiplier to obtain a 2% presentation per centimeter; and shift the oscilloscope trace to the left so that the second reference vertical pulse may be observed.

4. Rotate the VEL TC screwdriver adjustment on the module front panel to the center of its range and, with the VEL TC pushbutton depressed, adjust the internal VEL TC potentiometer (R16) so that the fourth tonewheel pulse falls within 1/8 centimeter of the second reference vertical pulse.

5. Stop the machine, remove the module extender, and replace the module in the machine.

Tonewheel Servo Gain

1. Ascertain that the following adjustments have been correctly made before proceeding with the servo gain adjustments:

a. 4XTW Frequency (tonewheel processor module, no. 313).

b. 4XTW Delay (tonewheel processor module).

c. Control Track Phase (head no. 1 centered over track no. 1).

2. Rotate the switch on the tape sync processor module (no. 317) to the PL position, and flip the toggle switch on the picture monitor so that the monitor will operate on external sync.

3. Remove one of the two wires connected to terminal 14 of terminal board 84TB1 located behind the PLAY control panel. (The removal of one of these wires is necessary to allow adjustment of the tonewheel servo in tape vertical alignment mode while at the same time preventing the machine from going into the pixlock servo mode.)

4. Operate the machine in the PLAY mode with manual guide servo control, and rotate the PB GUIDE POSITION control on the guide servo module (no. 221) clockwise to increase head tip penetration until the headwheel motor voltage is approximately 70 volts. *DO NOT EXCEED 70 VOLTS.*

5. Rotate the VEL GAIN screwdriver adjustment to a position which is approximately 25% in the counter-clockwise direction from its maximum clockwise position.

6. Rotate the PHASE GAIN screwdriver adjustment to obtain minimum horizontal jitter in the picture observed on the picture monitor, and readjust the VEL GAIN adjustment to obtain the best possible picture.

> NOTE: The picture should remain stable while the PB GUIDE POSITION control is rotated from maximum tip penetration (headwheel motor voltage of 70 volts) to minimum tip penetration (loss of picture), and horizontal jitter should not exceed 4 inches peak-to-peak on a monitor display 10 inches wide. (Return the control to its normal position after this check has been made.)

7. Depress the VEL TC pushbutton and note horizontal movement of the picture on the monitor. If necessary, readjust the VEL TC adjustment to obtain minimum horizontal roll.

8. Place the machine in the STOP mode, and replace the wire removed from terminal 14 of terminal board 84TB1 in step 3 above.

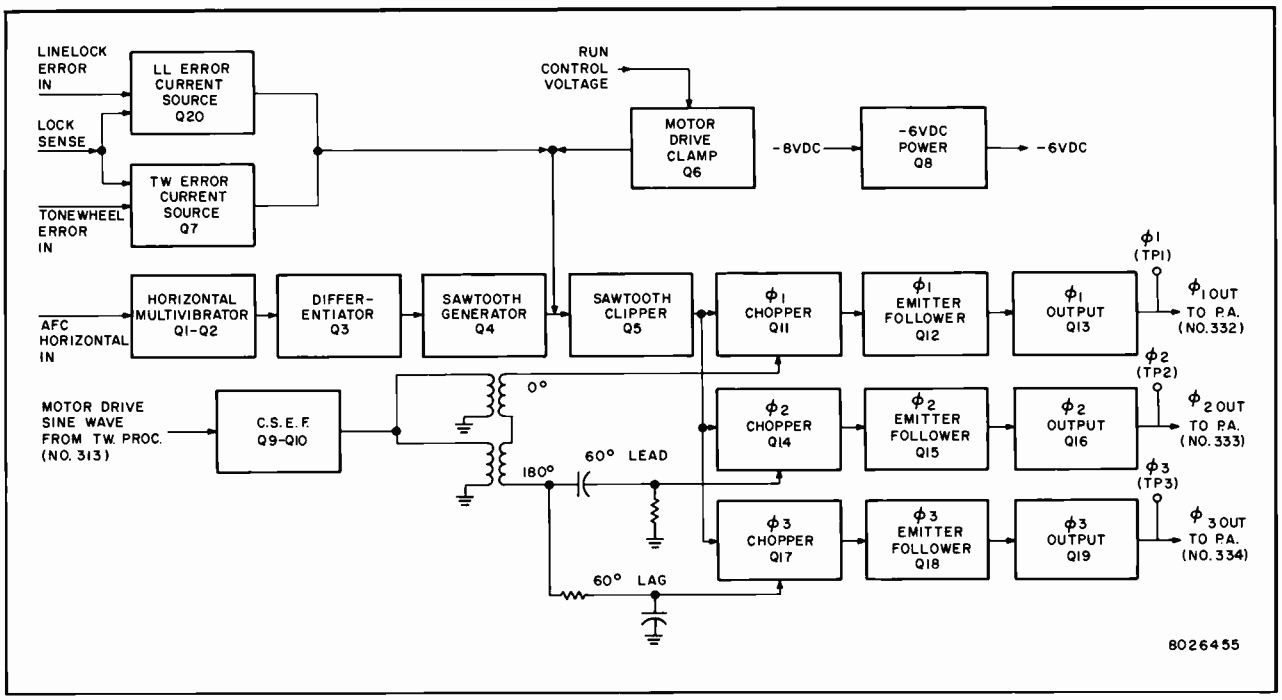


Figure 26—Headwheel Modulator Module Block Diagram

HEADWHEEL MODULATOR MODULE

Circuit Description

General

The headwheel modulator module (no. 315) receives a 480-cycle sinusoidal signal from the tonewheel processor module and converts it into three individual sinusoidal signals differing in phase by 120 degrees (figure 26). These signals are fed to separate power amplifier modules which furnish the power required to drive the headwheel motor. The headwheel motor speed is controlled by varying the amplitude of each individual signal in response to an input error signal.

Each 480-cycle sine wave signal is pulse modulated at a line-frequency rate (15,750 cps in domestic machines) by a chopper circuit. The width of the modulating pulse is determined by the magnitude of the input error signal from either the tonewheel or linelock error detecting circuits; thus the energy contained in each sinusoidal signal will be proportional to the error signal magnitude. The line frequency modulation information is then filtered out, leaving only the fundamental 480-cycle sine wave signal whose amplitude is a function of the energy remaining after modulation (see figure 27).

A second operation performed by the module circuitry is the generation of a negative 6 volts dc. This voltage is used in the headwheel modulator module, and is also fed to the tonewheel servo and linelock modules for use as a d-c reference voltage.

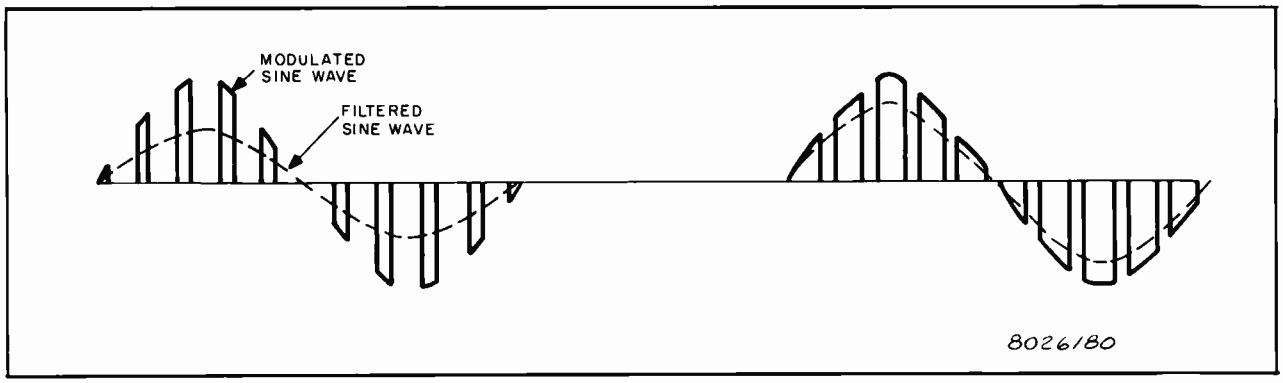


Figure 27—Variation in 480-Cycle Sine Wave Amplitude as Width of 15.75 kc Modulating Pulse Varies

Modulation Pulse Generator

Figure 28 shows the modulation pulse generator circuitry which generates a series of pulses at a horizontal rate to be utilized in modulating each of three 480-cycle sine wave signals before they are fed to the headwheel power amplifier modules. The modulation pulse width, which determines the resultant amplitude of each 480-cycle signal, is directly proportional to the magnitude of the error signal fed to the pulse generating circuits from the tonewheel error detecting circuits when the machine is operated in the tonewheel, switchlock, or TVA servo mode, or from the linelock error detecting circuits when the machine is locked in the pixlock servo mode.

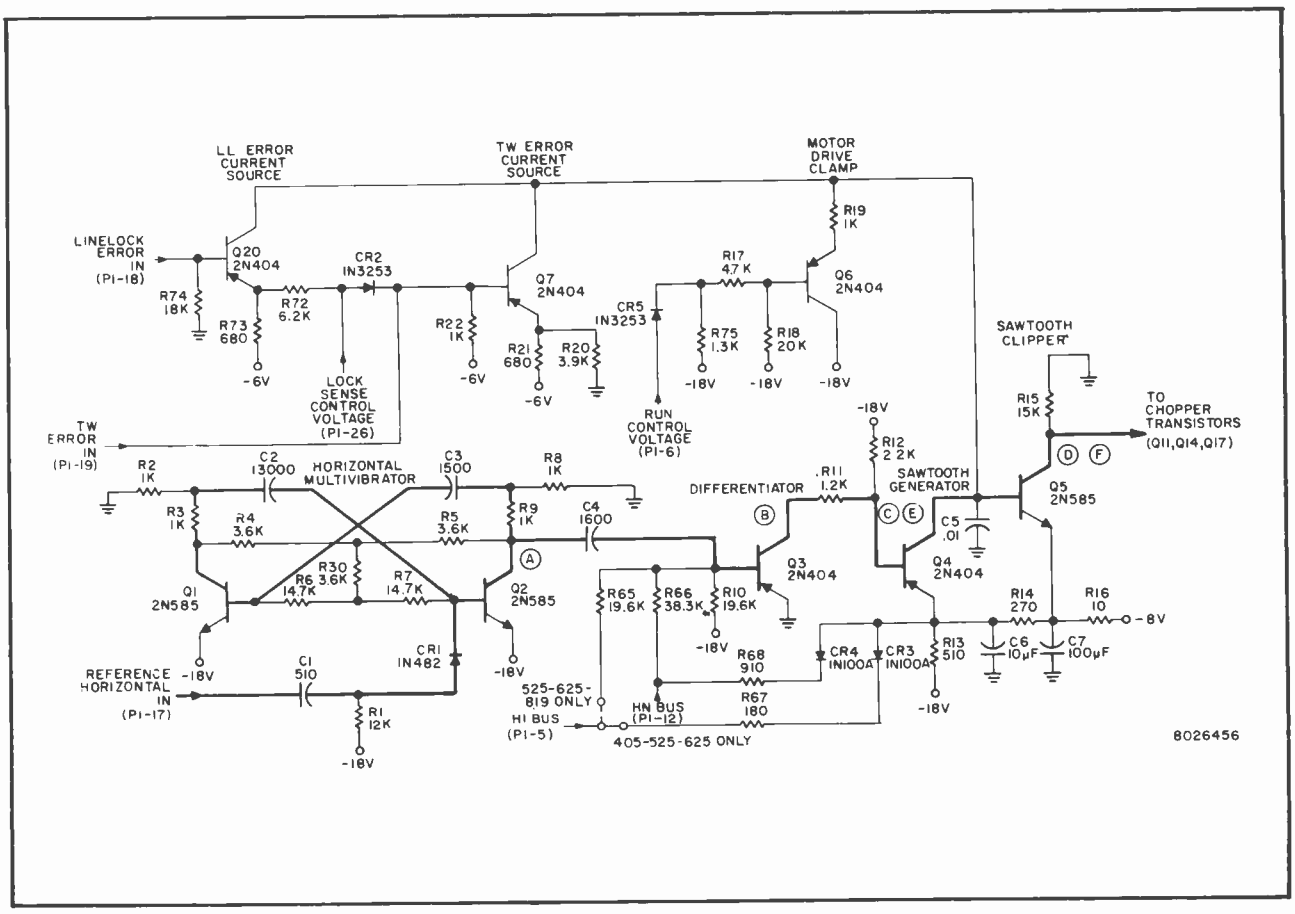
The reference horizontal signal, fed to the modulator module through pin 17 of plug P1 from the tape sync processor module (no. 317), is a negative pulse having an amplitude of approximately −18 volts (figure 28A). The pulse is differentiated by the network consisting of capacitor C1 and resistor R1, and the resulting positive-going pulse is fed through diode CR1 directly to the base of transistor Q2. Transistors Q1-Q2 and associated circuit components form the astable horizontal multivibrator having asymmetrical time constants. Due to the relative values of capacitors C2 and C3 in the multivibrator timing circuits, normal multivibrator operation is such that transistor Q2 will be cut off for a period which is approximately ten times that during which the transistor is saturated. Also, the total multivibrator period is greater than the period of one TV horizontal line, regardless of the line standard used. However, the positive-going triggering pulse fed to the base of transistor Q2 drives the transistor into saturation prematurely, thus ending the transistor "off" time so that the multivibrator period is made exactly equal to that of one TV horizontal line. The output waveform at the collector of transistor Q2 then appears as shown in figure 28A.

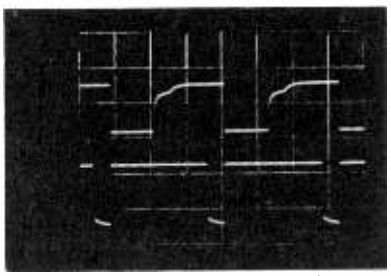
Capacitor C4 and resistors R10 and R65 or R66, depending upon the line standard used, form a network which differentiates the output waveform at the collector of transistor Q2 before it is fed to the base of transistor Q3 in the pulse-narrowing boxcar circuit. Transistor Q3, normally saturated, is cut off by the positive-going pulse resulting from the differentiation, and a narrow negative-going pulse then appears at its collector. The interval during which transistor Q3 is cut off, and therefore the width of the pulse at its collector, depends upon the value of the time constant network in its base circuit. This value is established by the time required for capacitor C4 to discharge through a resistance network to the negative potential which will cause transistor Q3 to be saturated once again. The resistance network in turn is determined by the line standard used, as shown in figure 29.

When the machine is to be used with 525/625/819-line standards only, resistor R65 is connected to the HI bus which is at ground potential during 525/625-line operation and at −20 volts dc during 819-line operation (figure 29, A and B). When the machine is to be used with 405/525/625-line standards only, there is no connection between the HI bus and resistor R65 (figure 29, C and D). In either set of standards, resistor R66 is returned to the potential on the HN bus. This potential is −20 volts dc during 525/625-line operation and ground during 405- or 819-line operation. As a result of the different time constant networks, transistor Q3 produces a negative-going pulse having a width which is inversely proportional to the line frequency rate. This allows the gain of the modulator circuitry to remain essentially constant, regardless of the line standard used, as will become apparent from the discussion below on the sawtooth generator circuit. Since the difference in frequency between 525- and 625-line standards is less than 1%, the width of the output pulse at the collector of transistor Q3 is the same for each standard as shown in figure 29, B and D.

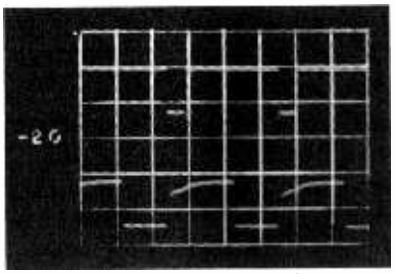
The narrow, negative-going output pulse at the collector of transistor Q3 (figure 28B) is fed to the base of transistor Q4 in the sawtooth generator circuit. During the interval between output pulses, the voltage divider network consisting of resistors R11 and R12 causes a negative bias voltage to be applied to the base of transistor Q4; however the potential at the emitter of Q4 is negative with respect to the base potential and the transistor is cut off. When the negative-going pulse appears at the base of transistor Q4 the transistor is driven into saturation. The potential at the collector of transistor Q4 then falls to that at its emitter, which in turn is established by the voltage divider network in the emitter circuit.

The voltage divider network in the emitter circuit of transistor Q4 consists of resistors R16, R14, R13, and either R67 or R68, depending upon the line standard used. When the machine is operated on 525/625-line standards the HN bus potential is −20 volts dc, thus forward biasing diode CR4. Resistor R68 is then essentially in parallel with resistor R13, and the emitter potential of transistor Q4 is approximately −12.5 volts dc. When the machine is operated on 405-line

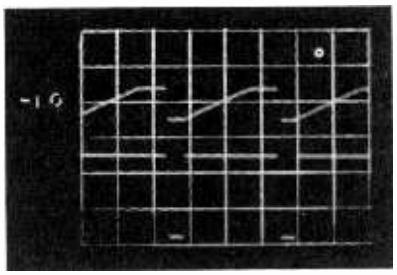




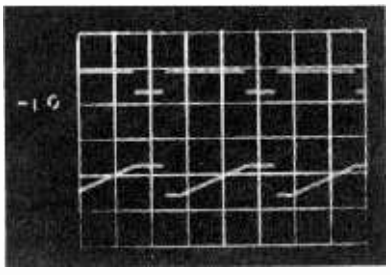
A. Top: Q2 collector, 10v/cm.
Bottom: P1-17 (REF HOR), 10v/cm.



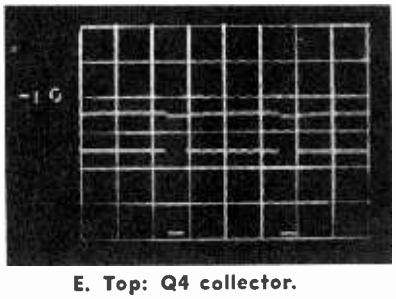
B. Top: Q3 collector, 10v/cm.
Bottom: Q2 collector, 10v/cm.



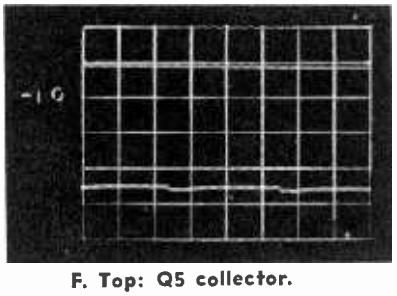
C. Top: Q4 collector.
Bottom: Q3 collector.
(STANDBY Mode)



D. Top: Q5 collector.
Bottom: Q4 collector.
(STANDBY Mode)



E. Top: Q4 collector.
Bottom: Q3 collector.



F. Top: Q5 collector.
Bottom: Q4 collector.

All sweep times 20 μsec/cm. Machine in STOP mode and amplitudes 5v/cm, unless otherwise noted.

Figure 28—Modulation Pulse Generator

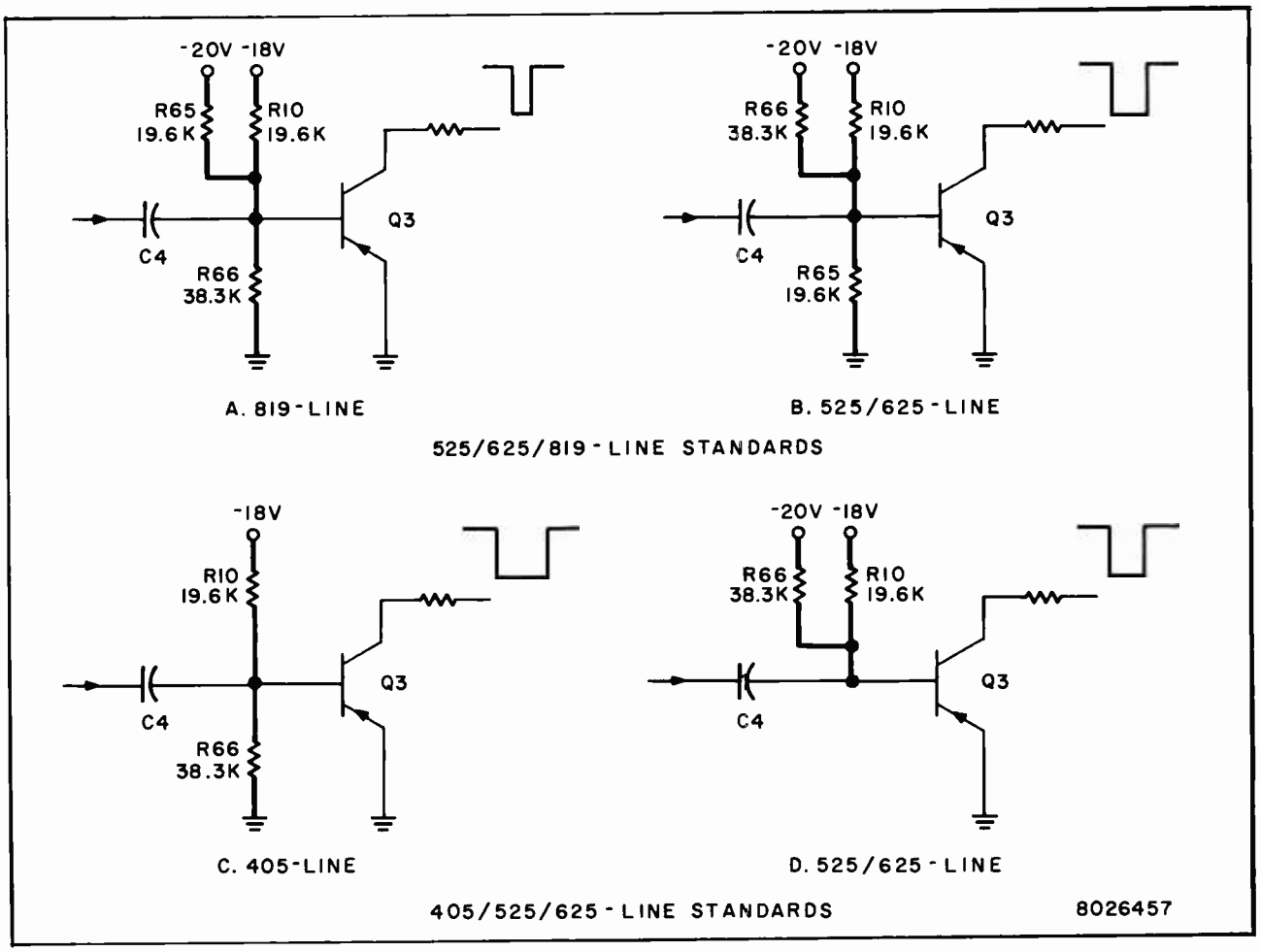


Figure 29—Transistor Q3 Biasing Networks as Determined by the Line Standard Used

standards the HI bus potential is −20 volts dc, thus forward biasing diode CR3. In this case resistors R67 and R13 are essentially paralleled, and the emitter potential falls to approximately −15 volts dc. If the machine is operated on 819-line standards there is no connection between the HI bus and resistor R67 and, in addition, the HN bus is at ground potential thereby reverse biasing diode CR4. The voltage divider network then consists of resistors R16, R14, and R13; thus the emitter potential is approximately −11.5 volts dc.

When transistor Q4 is driven into saturation, capacitor C5 charges rapidly to the collector potential of Q4 and holds this charge during the saturation interval, which is equal to the period of the output pulse from the boxcar circuit. At the instant transistor Q4 is cut off, capacitor C5 begins to discharge toward the base potential of current source transistor Q7 or Q20 as explained below. Due to the biasing arrangement in the emitter circuit of transistor Q4, the emitter potential increases in a positive direction

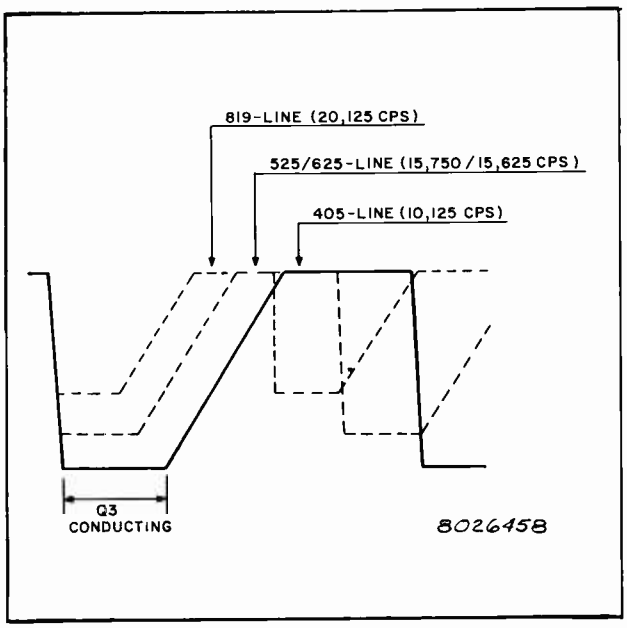


Figure 30—Trapezoid Waveforms Indicating Slopes Independent of Line Standards

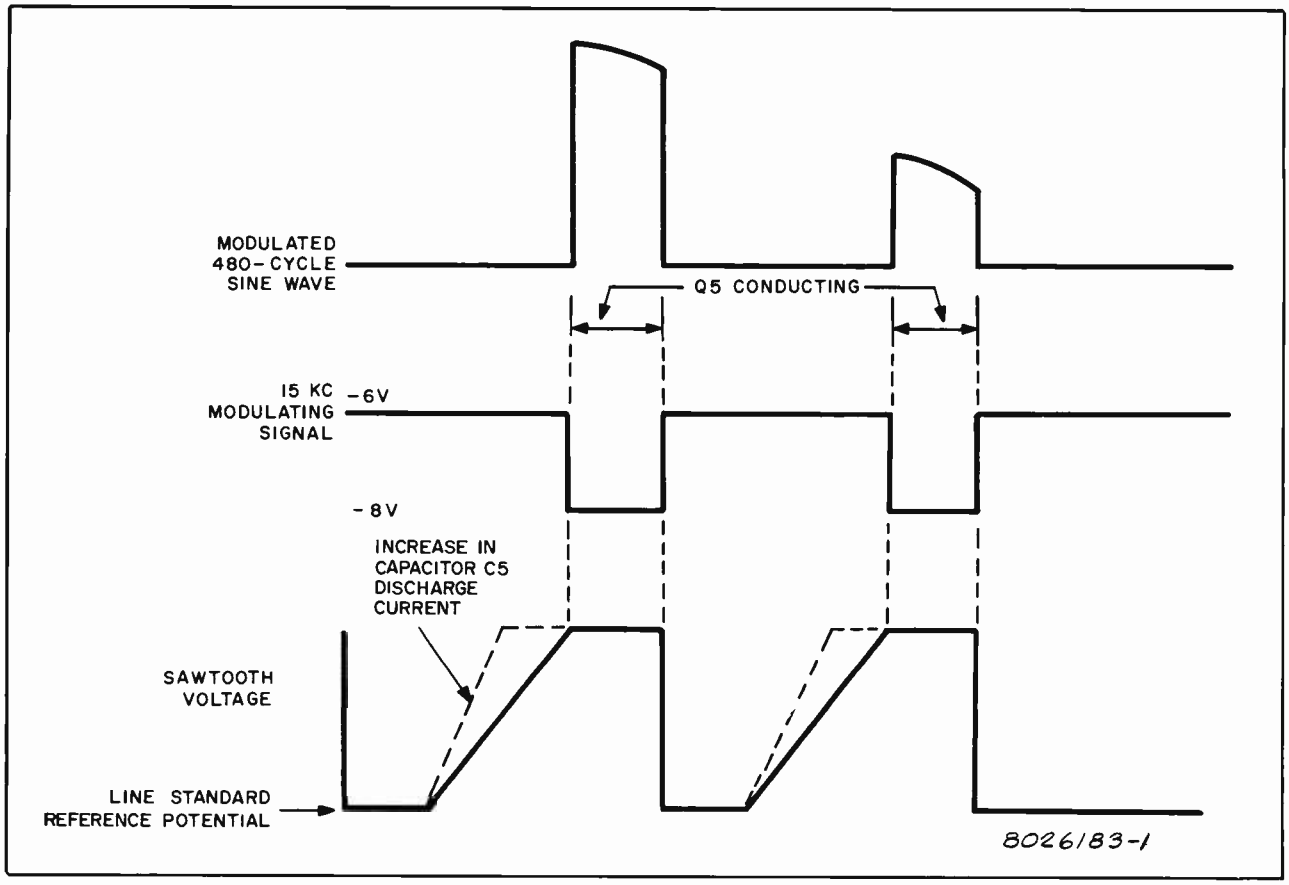


Figure 31—Effect of an Increase in Capacitor Discharge Current on the Sawtooth Voltage Waveform

(i.e., becomes less negative) as the line frequency increases. Therefore, the negative potential to which capacitor C5 charges is greatest for 405-line operation and least for 819-line operation. This arrangement, in conjunction with the fact that the width of the pulse at the collector of transistor Q3 is inversely proportional to the line frequency rate as mentioned above, insures that the slope of the sawtooth waveform will be essentially independent of the horizontal line frequency (figure 30). Thus the gain of the system is essentially constant for all line standards.

Clipper transistor Q5 is biased so that the transistor is cut off until capacitor C5 discharges to −8 volts dc, at which time the transistor is forced to conduct. When transistor Q5 is driven into conduction, its base is clamped at −8 volts and the sawtooth waveform is clipped, thus forming a trapezoidal waveform (figure 28C). Transistor Q5 will remain in a conducting state until the next horizontal pulse fed to the module again causes transistor Q4 to conduct and capacitor C5 to charge to the collector potential of Q4. While transistor Q5 is conducting, the bias potential at the bases of chopper transistors Q11, Q14, and Q17 is such that the transistors are cut off and will pass the 480-cycle sine wave motor voltages (figure 28D). Thus the time interval during which the 480-cycle signal is passed by the chopper transistors will be determined by the rate at which capacitor C5 discharges, and may be varied by increasing or decreasing this rate (figure 31).

The rate at which capacitor C5 discharges, and thus the slope of the trapezoid waveform, is controlled by the magnitude of the current provided by the applicable current source transistor as mentioned above. The choice of discharge path (current source transistor Q7 or Q20) depends upon the servo mode of operation, which in turn determines the potential provided by the lock sense control voltage. The lock sense control voltage, fed to the module through pin 26 of plug P1 from the tonewheel servo module, is −26 volts dc when the headwheel servo is in tonewheel or switch-lock mode, and when the machine has been switched to pixlock mode but before the actual "lock" has been attained (TVA mode). This voltage causes a negative

potential to appear at the emitter of transistor Q20 which cuts the transistor off, and reverse-biases diode CR2 so that transistor Q7 is biased into conduction. The tonewheel error signal, fed to the module through pin 19 of plug P1 from the tonewheel servo module, then determines the potential at the base of transistor Q7 and the transistor will provide the discharge current of capacitor C5 at a rate which depends upon the tonewheel error signal magnitude. When the machine has attained a "lock" in the pixlock mode of servo operation the lock sense control voltage is ground, thus forward biasing diode CR2. Transistor Q7 is then biased into cut-off and transistor Q20 is biased so that the linelock error signal, fed to the module through pin 18 of plug P1 from the linelock module, will cause Q20 to conduct and provide the discharge current of capacitor C5 at a rate which depends upon the linelock error signal magnitude. Resistor R74, returned to ground in the base circuit of transistor Q20, is provided to insure that transistor Q20 will remain cut off in the event of a loss in linelock error signal.

In any tape recorder RUN mode (i.e., any mode except STOP), the RUN bus is at ground potential. Diode CR5 is then forward biased and a negative potential of approximately −4 volts dc is applied to the base of motor drive clamp transistor Q6 from the voltage divider network consisting of resistors R17 and R18. However, the emitter potential of transistor Q6 cannot go any further in the positive direction than the clamping potential of transistor Q5 (−8 volts dc) and thus the transistor is cut off and has no effect on the modulation pulse generator circuits. When the machine is in the STOP mode, the RUN bus is at −26 volts dc and diode CR5 is reverse-biased. Resistors R75, R17, and R18 then form a voltage divider network which applies a bias potential of approximately −17.5 volts dc to the base of transistor Q6 and the transistor is driven into conduction. When transistor Q6 conducts, its emitter potential falls to approximately −19 volts and, since this potential is applied to the base of transistor Q5, it cuts Q5 off. Thus chopper transistors Q11, Q14, and Q17 are biased into conduction continuously and there will be no output to the power amplifier modules. Figures 28E and 28F show the waveforms at the collectors of transistors Q4 and Q5 respectively, with the machine in the STOP mode.

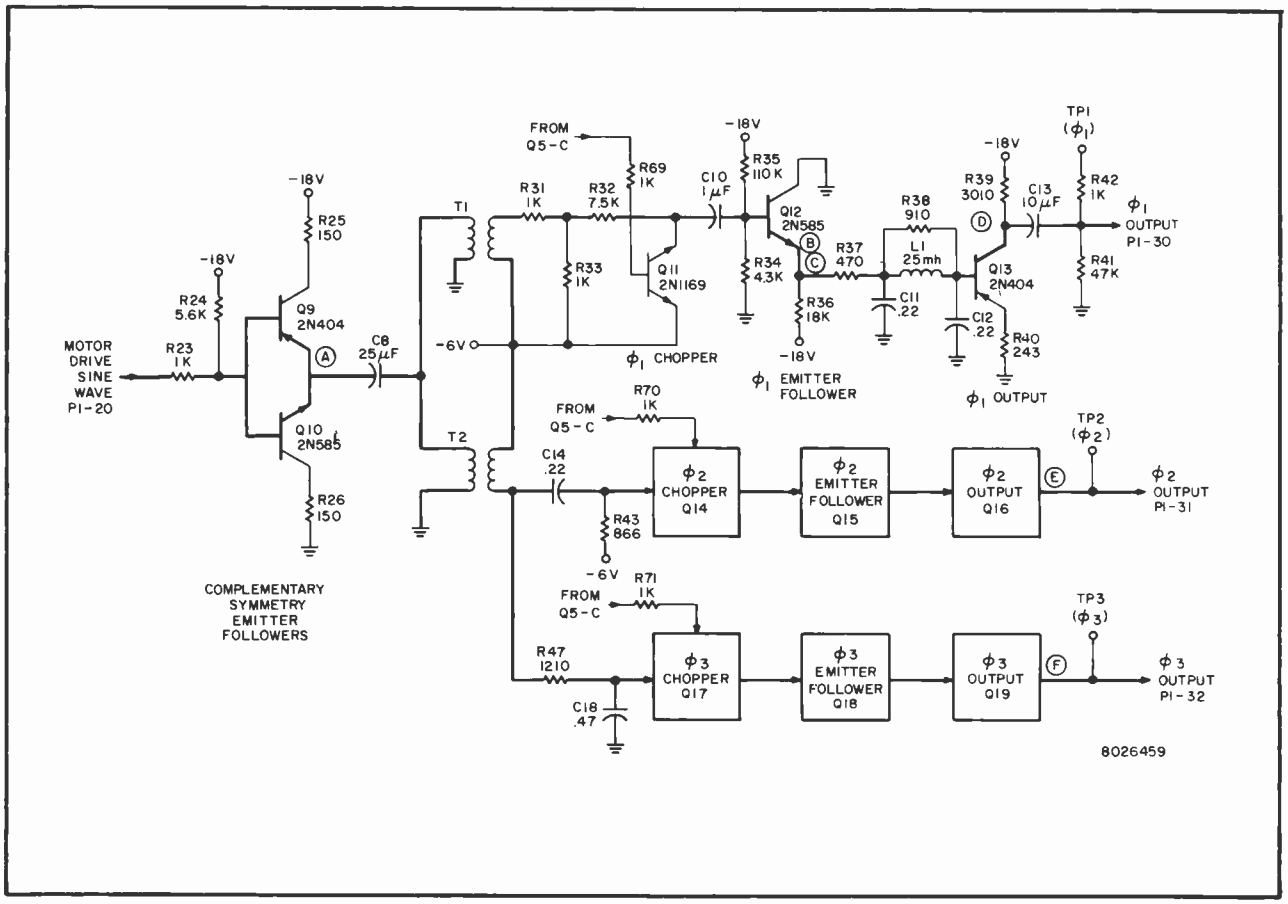
Modulators and Amplifiers

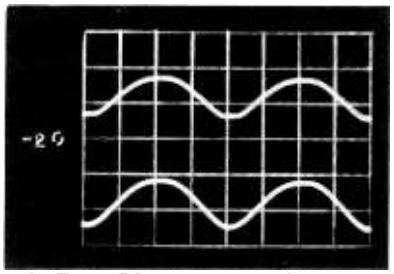
The 480-cycle motor drive sine wave signal, having an amplitude of approximately 13 volts peak-to-peak, is fed to the module through pin 20 of plug P1 from the tonewheel processor module (no. 313). Normally, the tonewheel processor module produces this signal in any mode of machine operation, including the STOP mode. However, if there is an open circuit between the tonewheel head and the tonewheel processor module, the fault sensor circuit in the module prevents formation of the signal and thus there is no input to the headwheel modulator module. In the STOP mode, the headwheel motor is prevented from running by the action of transistor Q6 as explained in the modulation pulse generator description above.

Complementary symmetry emitter follower transistors Q9-Q10 reduce the impedance of the input 480-cycle signal and thereby provide sufficient current gain to drive the phase splitter transformers T1 and T2. Transformers T1 and T2, driven by the 480-cycle output signal from transistors Q9-Q10 (figure 32A), have their primary windings connected in parallel and their secondary windings connected in series. This arrangement causes the output signal from transformer T1 to be in phase with the input signal, and the output signal from transformer T2 to be shifted 180 degrees in phase with respect to the input signal. The 480-cycle signal at the secondary of transformer T1 is then fed through a resistive network to chopper transistor Q11, while the signal at the secondary of transformer T2 is subjected to further phase shifting by differentiating and integrating networks before being applied to chopper transistors Q14 and Q17.

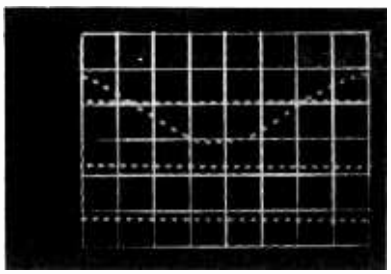
Capacitor C14 and resistor R43 form a differentiating or phase "lead" network and the component values are such that the 480-cycle signal is advanced 60 degrees. The integrating or phase "lag" network consists of resistor R47 and capacitor C18, and the values of these components cause a 60 degree retardation. As a result of the phase shifting networks, the original 480-cycle input signal is split into three signals differing in phase by 120 degrees. Each signal continues in a separate path through a chopper, emitter follower, and output circuit. The circuits in the ϕ_1 signal path are described below and the operations performed on the ϕ_2 and ϕ_3 signals, which follow paths parallel to that of the ϕ_1 signal, are identical.

The 480-cycle sinusoidal signal at the secondary of transformer T1 is fed to chopper transistor Q11. Since the bottom of the secondary winding is connected to −6 volts dc, on alternate half-cycles the 480-cycle signal will go either positive or negative with respect

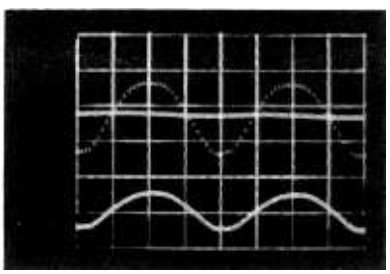




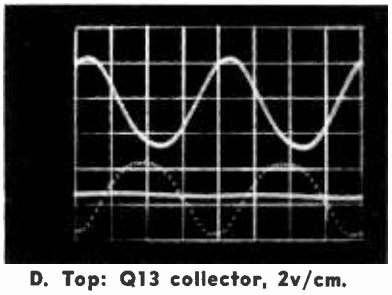
A. Top: Q9 emitter, 10v/cm.
Bottom: P1-20 (MOTOR DRIVE SINE WAVE), 10v/cm.



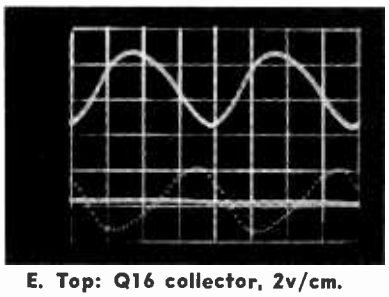
B. Top: Q12 emitter, 1v/cm.
Bottom: Q5 collector, 2v/cm.
(200 μsec/cm)



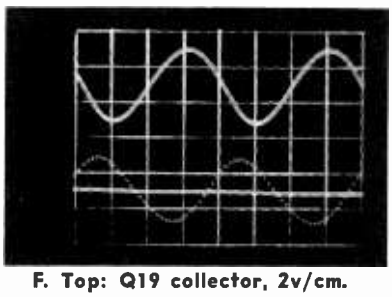
C. Top: Q12 emitter, 1v/cm.
Bottom: Q9 emitter, 10v/cm.



D. Top: Q13 collector, 2v/cm.
Bottom: Q12 emitter, 1v/cm.



E. Top: Q16 collector, 2v/cm.
Bottom: Q15 emitter, 1v/cm.



F. Top: Q19 collector, 2v/cm.
Bottom: Q18 emitter, 1v/cm.

Machine in STANDBY mode. All sweep times 500 μsec/cm, unless otherwise noted.

Figure 32—Modulator and Amplifier Circuits

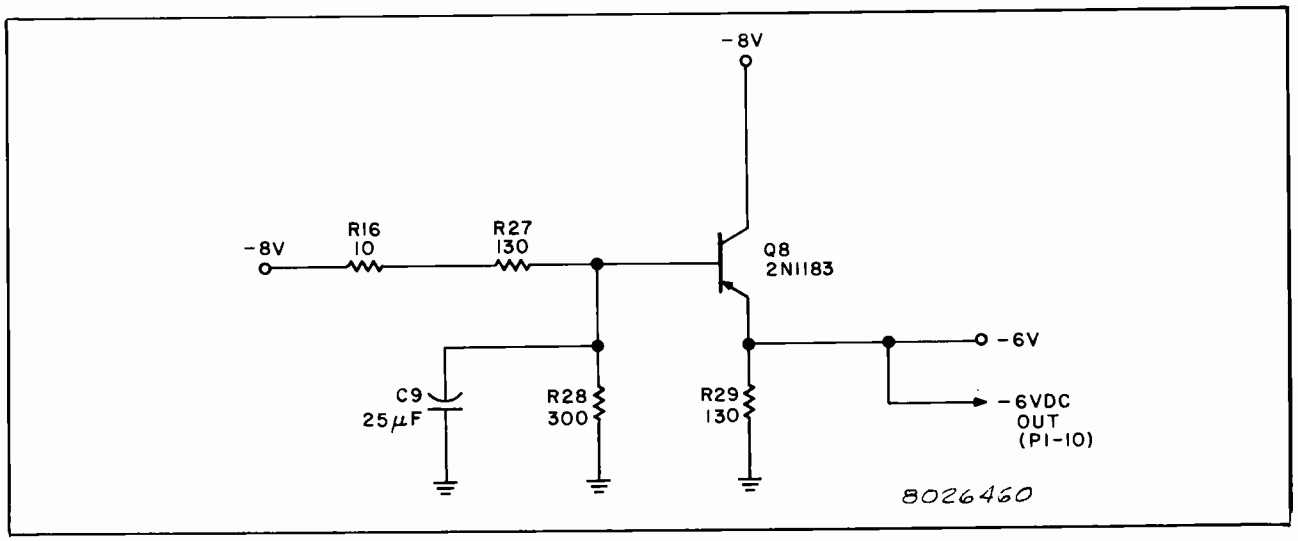


Figure 33— −6 Volt DC Power Circuit

to this voltage. Therefore, to obtain proper modulation (chopping action) on both positive and negative half-cycles, a bilateral transistor is used. In this particular type transistor, identical operation will be obtained with either electrode acting as the collector.

Referring to figure 32, when the input 480-cycle signal causes the top of the secondary winding of transformer T1 to go positive with respect to −6 volts dc the bottom goes negative, and thus the lower electrode of chopper transistor Q11 acts as the emitter and the upper electrode as the collector. When the polarity of the 480-cycle signal reverses, the lower electrode of Q11 acts as the collector and the upper electrode as the emitter. During the interval between output pulses from transistor Q5, which occur at a horizontal rate (15.75 kc in domestic machines), the base potential of transistor Q11 is −6 volts dc. This causes transistor Q11 to conduct and thereby clamp the 480-cycle signal at −6 volts. Resistor R32, in series with the secondary winding of transformer T1, raises the impedance of the 480-cycle signal so that the signal is effectively shorted out by the very low impedance of transistor Q11. When transistor Q5 produces an output pulse, the base potential of Q11 falls to −8 volts dc thus cutting the transistor off, and the 480-cycle signal is allowed to pass to the base of transistor Q12. (Resistors R69, R70, and R71 in the base circuits of transistors Q11, Q14, and Q17 insure that the distribution of base current to each transistor is approximately equal.)

Transistor Q12, operating as an emitter follower, isolates the modulation generator circuits from the low-pass filter network consisting of resistor R38, coil L1, and capacitors C11 and C12. The signal at the emitter of transistor Q12 is a series of pulses occurring at a 15.75 kc rate, modulated by the 480-cycle signal (figures 32B and 32C). The filter network removes the 15.75 kc component from the composite signal and produces a 480-cycle sinusoidal signal whose amplitude is directly proportional to the modulating pulse width. The filtered signal is amplified by output transistor Q13 and fed through pin 30 of plug P1 to a power amplifier module (no. 332) as the ϕ_1 output signal. Test point TP1 (ϕ_1) is provided for convenience in observing the ϕ_1 output signal, which appears as shown in figure 32D. The a-c and d-c bias of the output circuit is firmly established by one-percent resistors (R39 and R40), placed in the emitter and collector circuit of output transistor Q13.

The ϕ_2 and ϕ_3 output signals are developed in a manner identical to that described above for the ϕ_1 output signal. These signals may be observed at test points TP2 (ϕ_2) and TP3 (ϕ_3), and are shown in figures 32E and 32F respectively.

−6 Volt DC Power

The −6 volt dc power circuit produces an essentially constant negative 6 volt output for use in this module as well as in the tonewheel servo and linelock modules (nos. 314 and 316). As shown in figure 33, transistor Q8 is connected across the voltage divider network consisting of resistors R16, R27, and R28. Thus the potential at the base of transistor Q8 (approximately −6 volts dc) will remain constant and, because of the insignificant voltage drop between the emitter and base of Q8, the emitter potential will also remain constant for designed variations in load current.

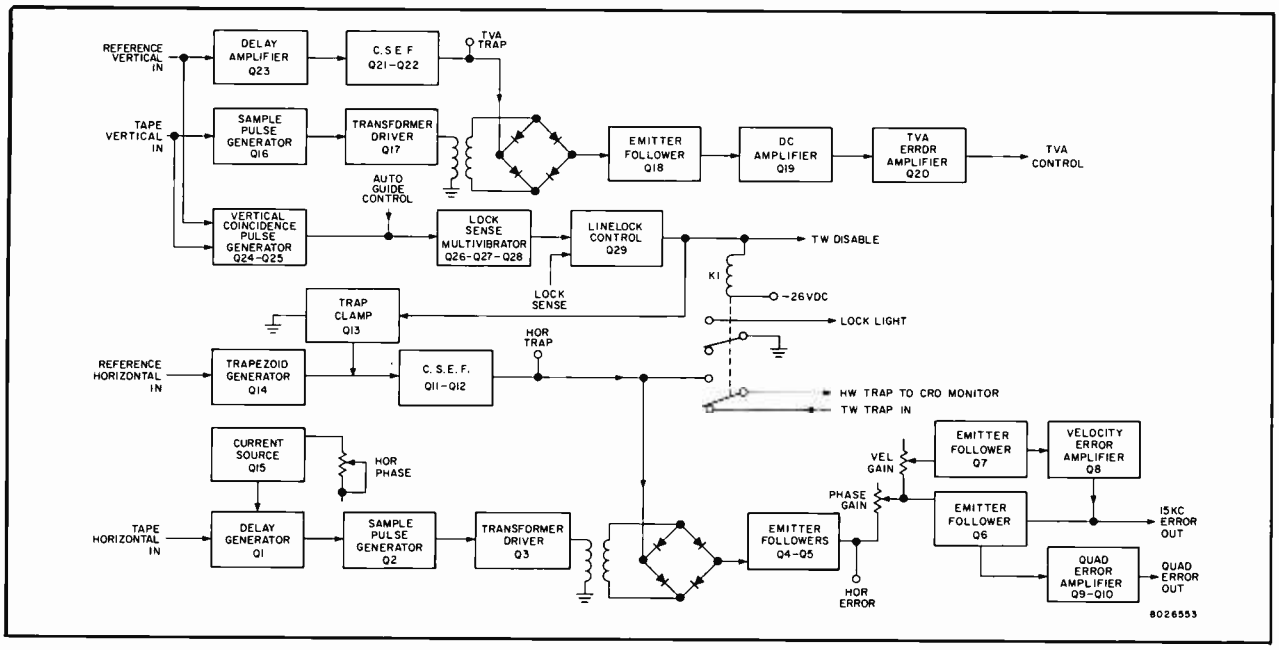


Figure 34—Linelock Module Block Diagram

LINELOCK MODULE

Circuit Description

General

In the pixlock mode of servo operation, the playback picture is phased so that vertical and horizontal tape sync is timed with the vertical and horizontal reference sync obtained from the local sync generator. Vertical sync timing is accomplished by the switch-lock function in conjunction with the tape vertical alignment (TVA) servo loop. When the sync signals have been aligned, this fact is detected by a lock sense circuit and control of the headwheel motor speed is transferred from the tonewheel servo (TVA mode) to the linelock servo for a more precise control of the motor speed.

The linelock module (no. 316) performs three basic functions essential to precise control of the headwheel motor speed when the machine is switched to the pixlock mode of servo operation during tape playback. These functions are the generation of (1) the TVA control voltage; (2) the lock sense control voltage; and (3) the 15 kc error signal. The various circuits utilized in performing these functions are shown on the block diagram, figure 34.

The TVA control voltage is obtained from a servo loop which utilizes the comparison of tape and reference vertical sync signals to develop an error signal when the machine is switched to the pixlock mode of servo operation, but prior to an actual "lock". The error signal thus developed controls circuitry in the reference generator module (no. 312) which generates a timing correction in the tonewheel servo reference phase sample pulse path to attain tape and reference vertical sync alignment. This timing correction is required because the tonewheel servo loop acting alone controls only the tonewheel phase with respect to the local reference. Since the proposed SMPTE standard allows a one line variation of the vertical signal location on the tape, it would be possible for the tape vertical sync to differ from the reference vertical sync by as much as one line. If this occurs, switching to the pixlock mode would cause the machine to "lock-up" one line off, since the linelock function controls the headwheel motor speed by comparing the tape horizontal sync to the reference horizontal sync. Also, it is sometimes necessary to play back tapes where the vertical sync location on the tape exceeds the proposed SMPTE standard. Therefore, the TVA servo loop senses the location of tape vertical sync, compares it to reference vertical sync, and provides the error signal necessary to modulate the reference phase sample pulse in the tonewheel servo loop so that tape and reference vertical signals will be aligned to within ± 15 microseconds. When vertical alignment has been attained, the lock sense circuit automatically switches headwheel motor control from the tonewheel to the linelock servo.

The lock sense circuit performs this switching function by utilizing a coincidence gate in sensing the instant when tape and reference vertical sync signals are closely aligned. The resulting control voltage

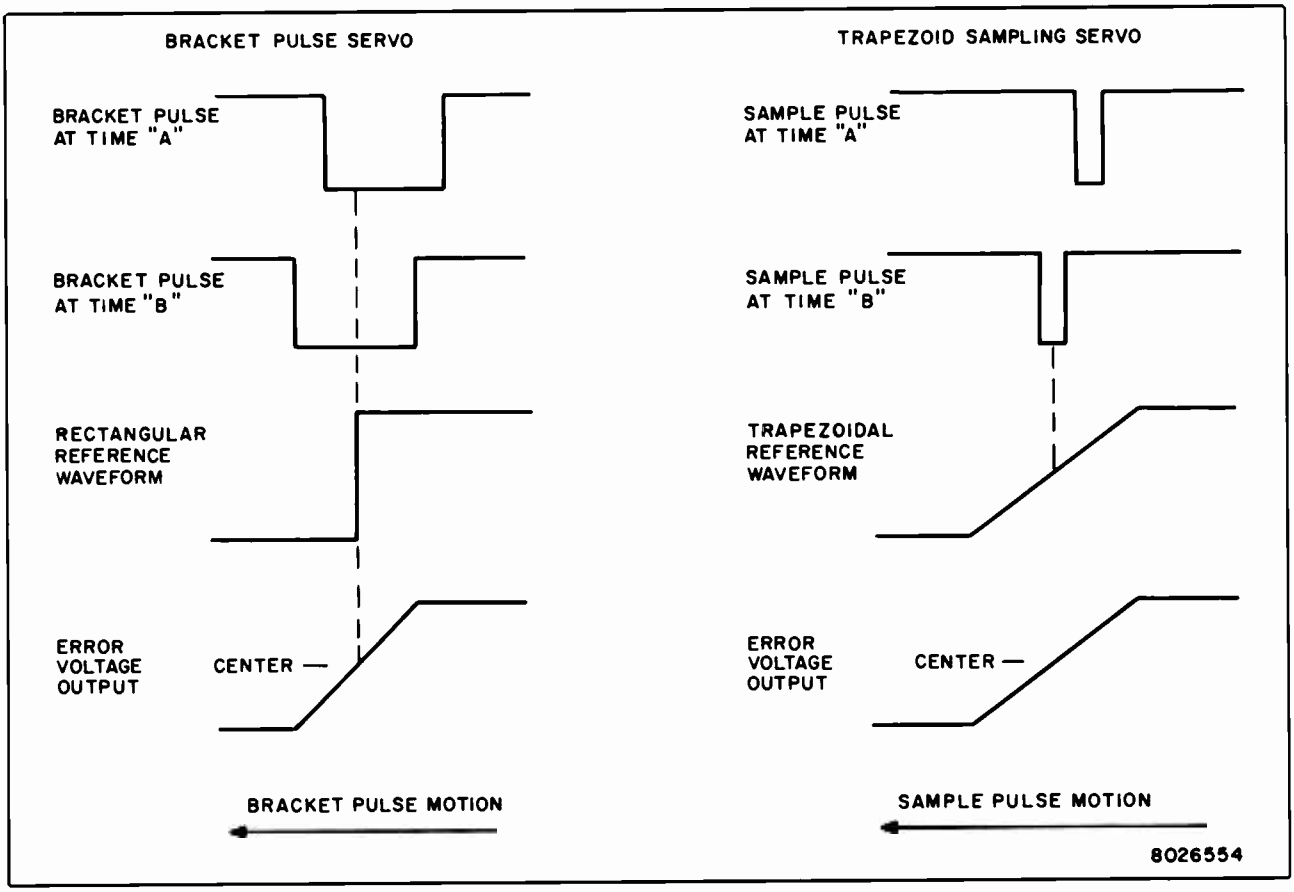


Figure 35—Bracket Pulse and Trapezoid Sampling Servo Waveforms

enables the linelock servo to provide the headwheel modulator module with the error signal which controls the headwheel motor speed; while at the same time it prevents the tonewheel error signal from presenting conflicting information to the modulator module.

When a "lock" has been attained, the linelock servo performs the third module function mentioned above. This function is the actual control of the headwheel motor speed by an error signal which is developed when a reference trapezoid waveform, generated from reference horizontal sync, is sampled in a comparator bridge circuit by a pulse generated from tape horizontal sync. Sampling in this servo is at a line frequency rate so that its error response, limited principally by the motor inertia, will be much more rapid than that of the tonewheel servo, thus resulting in tighter control of the headwheel motor speed. Velocity information is obtained from the "velocity loop" of the linelock servo by differentiating the phase error signal. The differential of the phase (rate of change of phase, $d\phi/dt$) is equivalent to velocity. Velocity information thus obtained may be a-c coupled, since only rate information is desired. This method of obtaining velocity information, resulting in a much simpler circuit than the tonewheel servo velocity loop, can be used here because the headwheel motor is already running at approximately the correct speed, and only comparatively slight variations in speed must be detected. Since the tonewheel servo has the more stringent requirement that the headwheel motor must be started from STOP mode, this method of obtaining velocity information cannot be used in the tonewheel velocity loop because a simple differentiating circuit would give no rate information for a constant speed of zero.

Tape Vertical Alignment (TVA) Servo

The function of the tape vertical alignment (TVA) servo loop is to align the tape vertical sync pulses with the reference vertical sync pulses, thereby permitting an actual "lock" in the pixlock mode of servo operation. Thus the tape and reference vertical sync pulses will be properly aligned when the linelock function gains control of the headwheel system.

The TVA servo loop differs slightly from the other headwheel system servo loops in its method of sampling. In the other loops, the reference signal generates a sloping waveform, i.e. a sawtooth or trapezoid

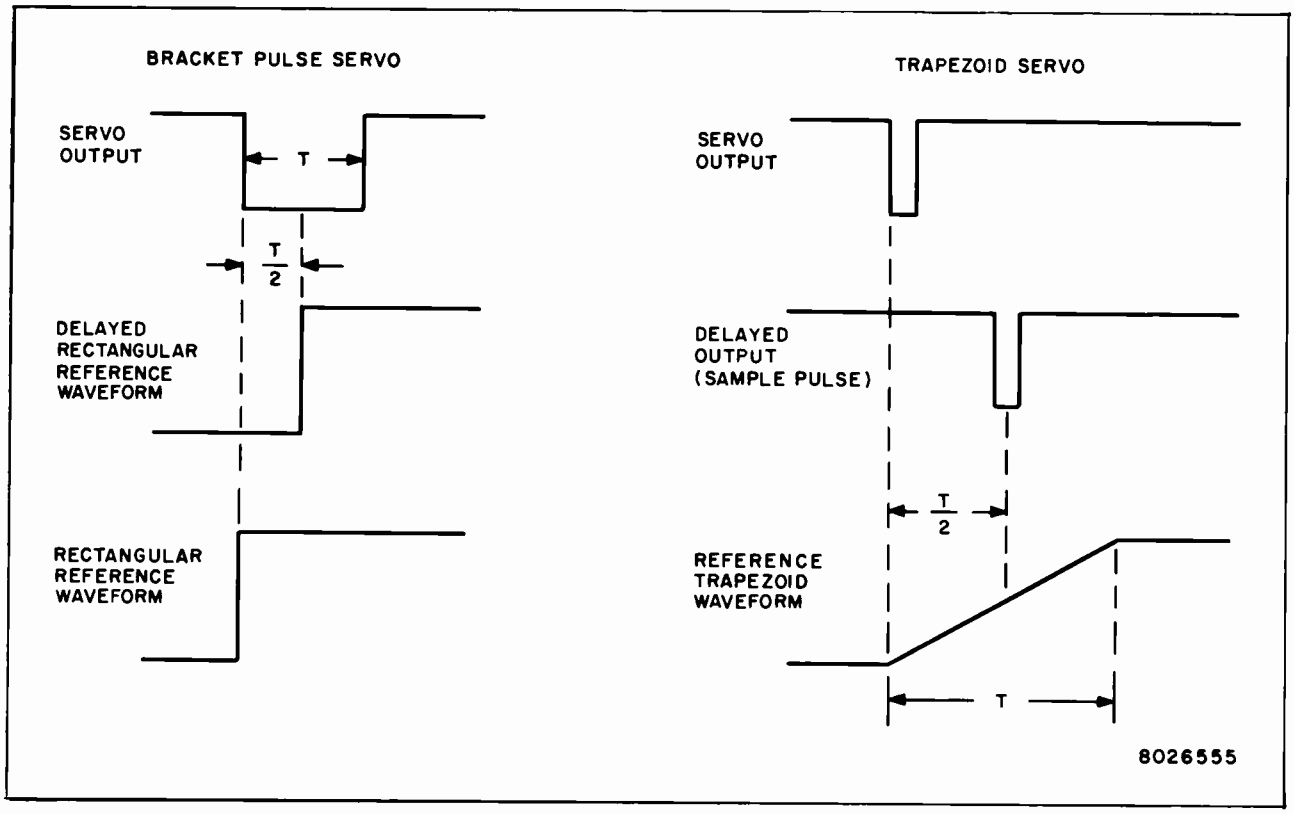


Figure 36—Half-Pulse and Half-Slope Delays

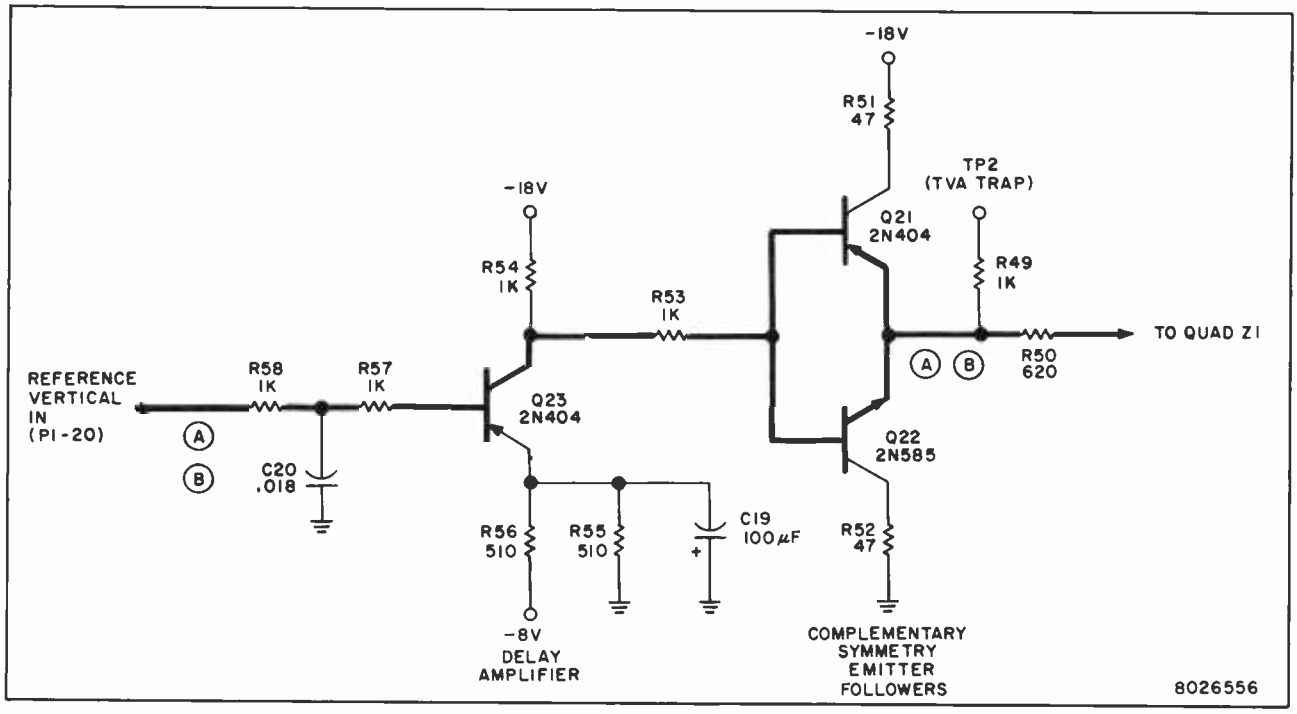
(truncated sawtooth), and the signal to be controlled generates a narrow pulse which samples the sloping waveform. The error voltage output is then a function of the sampling pulse position relative to the sloping waveform.

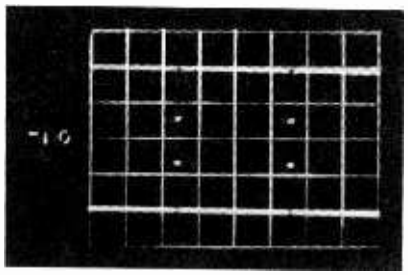
In the TVA servo loop however, the reference signal generates a rectangular waveform and the signal to be controlled generates a pulse (called the "bracket" pulse) which "brackets" the edge of the rectangular waveform. As shown in figure 35, sampling during the interval of the bracket pulse occurs partly on the more positive portion of the rectangular reference waveform and partly on the more negative portion. Therefore, the error voltage output will be a resultant of the length of time during which the bracket pulse samples the more positive and more negative portions of the rectangular waveform. As the bracket pulse moves from right to left in figure 35, the error voltage becomes increasingly negative. Figure 35 also shows that the error voltage output, as a function of the controlled signal, is the same for either the bracket pulse servo or the trapezoid sampling servo. In either case, when the loop is closed the servo will "lock-up" to the point where the error voltage output is equivalent to the voltage at the center of the trapezoid slope. Under this condition, the sampling pulses will be located as shown in the second line of figure 35.

In the bracket pulse servo, the leading edge of the sample (bracket) pulse *precedes* the leading (timed) edge of the rectangular reference waveform. However, in the trapezoid servo, the leading edge of the sample pulse *follows* the beginning (timed edge) of the reference trapezoid slope. Since in either sampling method it is desired that the input signals which form the sample pulse and reference waveform be aligned, a delay must be introduced into one path. In the bracket pulse servo, the *reference waveform* is delayed with respect to the input pulse which formed it, by an interval equal to one-half the bracket pulse period (half-pulse delay). In the trapezoid servo, the *sample pulse* is delayed with respect to the input pulse which formed it, by an interval equal to one-half the trapezoid slope (half-slope delay). (See figure 36.)

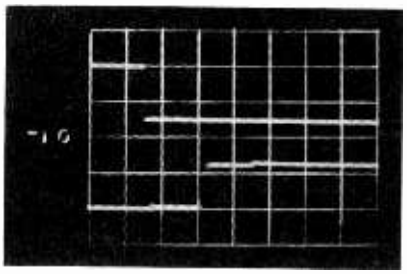
A. Reference Vertical Delay Generator

In the linelock module the TVA rectangular reference waveform is developed from the reference vertical pulse which is fed to the module through pin 20 of plug P1 from the reference generator module (no. 312). The reference vertical pulse is negative-going with an amplitude of approximately 8 volts (figure 37A) and occurs at a 60-cycle rate (50-cycle rate in International machines). Resistor R58 and capacitor





A. Top: P1-20 (REF VERT), 5v/cm.
Bottom: Q21 emitter, 10v/cm.
(5 msec/cm)



B. Top: P1-20 (REF VERT), 5v/cm.
Bottom: Q21 emitter, 10v/cm.
(10 μsec/cm)

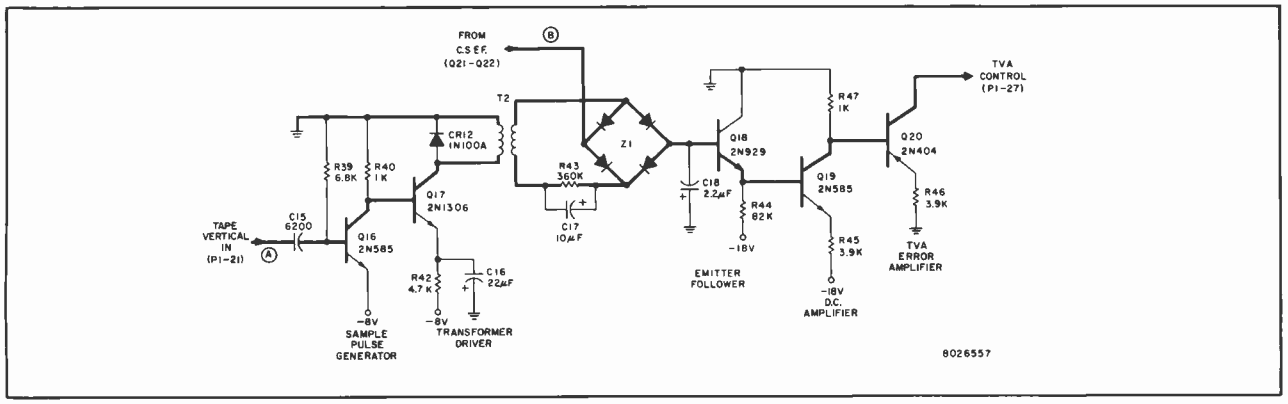
Machine in PLAY/PL mode.

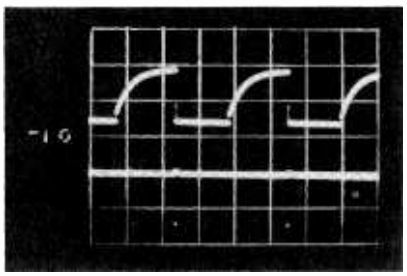
Figure 37—Reference Vertical Delay Generator

C20 form an integrating network which integrates the reference vertical pulse before it is fed to the base of delay amplifier transistor Q23.

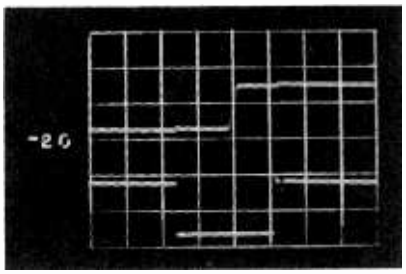
Transistor Q23 has a potential of approximately −4 volts dc at its emitter, due to the action of the voltage divider network consisting of resistors R55 and R56, and the transistor is normally cut off. When the potential of the integrated vertical reference pulse goes more negative than −4 volts, transistor Q23 conducts and produces a positive-going pulse at its collector. Thus the positive-going pulse, or rectangular reference waveform, is delayed with respect to the vertical reference pulse by an interval which is determined by the time required for capacitor C20 to charge to −4 volts through resistor R58. This interval (approximately 15 microseconds) is the half-pulse delay of the bracket pulse servo, and is in turn established by the amplitude of the input reference vertical pulse and the values of C20 and R58 together with the bias voltage established at the emitter of transistor Q23.

Complementary symmetry emitter follower transistors Q21-Q22 lower the impedance of the rectangular reference waveform and provide the current gain required to drive comparator quad Z1. The rectangular reference waveform may be observed at test point TP2 (TVA TRAP) and is shown in figure 37A (bottom). Figure 37B shows the relationship between the incoming reference vertical pulse and the delayed reference waveform. The delay indicated in figure 37B is the half-pulse delay mentioned above and shown in figure 36.





A. Top: P1-21 (TAPE VERT).
Bottom: Q17 collector.
(5 msec/cm)



B. Top: Q21 emitter, 10v/cm.
Bottom: Q17 collector.
(10 μsec/cm)

Machine in PLAY/PL mode. All amplitudes 5v/cm, unless otherwise noted.

Figure 38—Bracket Pulse Generator and Error Detector

B. Tape Vertical Bracket Pulse Generator and Error Detector

The tape vertical bracket pulse, used in the TVA servo loop to sample the edge of the rectangular reference waveform, is developed from the vertical square wave multivibrator output in the tape sync processor module (no. 317). The tape vertical waveform, appearing as shown in figure 38A, is applied to the module at pin 21 of plug P1 and drives the sample pulse generator transistor Q16.

Transistor Q16 and associated circuit components form a boxcar circuit, and with no signal applied to the base of the transistor it is biased into saturation. The negative-going edge of the incoming tape vertical waveform drives Q16 into cut-off, and its collector potential immediately rises toward ground until it reaches a level which allows transformer driver transistor Q17, normally cut off, to conduct. As transistor Q17 conducts, it clamps the collector of transistor Q16 at this level for an interval which is determined by the values of resistor R39 and capacitor C15. The actual level at which the collector of transistor Q16 will be clamped depends upon the bias voltage developed at the emitter of transistor Q17. This voltage in turn is determined by the repetition rate (60 cps in domestic machines; 50 cps in International machines) and pulse duration of the output from transistor Q16, as well as by the current required by pulse transformer T2. Thus the resulting output at the collector of transistor Q17 is the narrow, negative-going bracket pulse (figure 38A, bottom) whose width is determined by the values of resistor R39 and capacitor C15 in the boxcar circuit of transistor Q16, and also by the amplitude of the incoming tape vertical pulse. Transistor Q17 provides the current gain required to drive pulse transformer T2, and diode CR12 is inserted into the collector circuit of Q17 to suppress the inductive kick-back of the transformer.

Transformer T2 splits the bracket pulse phase and drives opposite ends of the comparator quad Z1, as shown in figure 38. The quad is also driven by the rectangular reference waveform whose formation is described above in the *Reference Vertical Delay Generator* discussion. During the bracket pulse interval the diodes of the quad are forward biased, thus providing a low impedance path between storage capacitor C18 and the complementary symmetry emitter follower transistors Q21-Q22. Therefore, during the bracket pulse interval capacitor C18 may charge or discharge to a potential which is the resultant of the duration of the positive and negative portions of the rectangular reference waveform from Q21-Q22. Fig-

ure 38B shows the bracket pulse and reference waveform with the machine operating in the pixlock servo mode.

During the interval between bracket pulses, the diodes are cut off and capacitor C18 is disconnected from the complementary symmetry emitter follower transistors. The capacitor then discharges slightly through the very high input impedance of emitter follower transistor Q18; however, the time constant of the discharge path is so great that the potential established during sampling will be held essentially constant during the remainder of the interval between bracket pulses.

The voltage developed across capacitor C18 is fed to emitter follower transistor Q18, and the signal at the emitter of Q18 is then applied to the base of d-c amplifier transistor Q19. Transistor Q19 amplifies the error voltage before it is fed to transistor Q20 which acts as a current source. The TVA error current thus developed is fed from pin 27 of plug P1 to the reference generator module (no. 312) where it is utilized in a timing network to control the width of the pulse output from a boxcar circuit (transistor Q17). The operation of the boxcar circuit is such that it acts as a variable delay in the tonewheel servo phase reference pulse path, and this delay is instrumental in aligning the tape and reference vertical sync pulses. Thus in the pixlock servo mode, prior to attaining a "lock", the delay is dependent upon the current provided by TVA error amplifier transistor Q20 which in turn is controlled by the error voltage developed across capacitor C18.

Vertical Coincidence Pulse Generator and Lock Sense Control

The transition from tonewheel to linelock (pixlock) control of the headwheel motor speed is automatic, and the circuit which senses the condition when tape and reference vertical sync signals are closely aligned is designated the lock sense circuit. The lock sense circuit provides a control voltage which automatically switches particular circuits in this module, the tonewheel servo, and the headwheel modulator modules, from tonewheel to linelock servo operation when tape and reference vertical sync coincidence occurs.

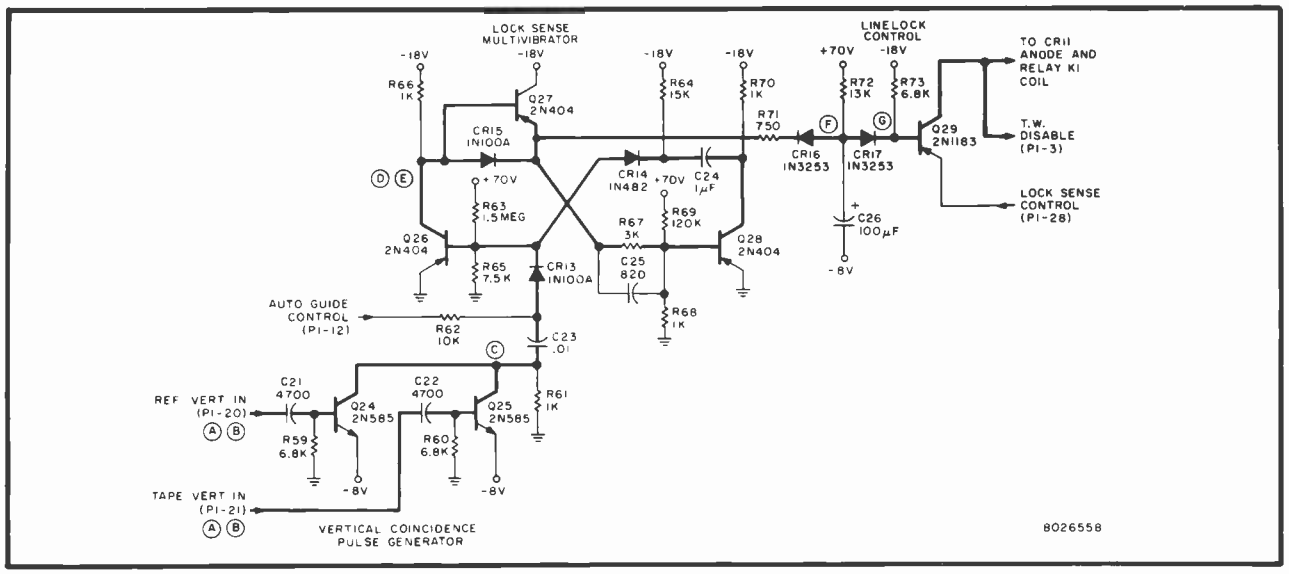
The reference vertical pulse from the reference generator module, used in developing the rectangular reference waveform in the TVA servo loop, is also fed to vertical coincidence pulse transistor Q24. Similarly, the tape vertical waveform from the tape sync processor module, used in developing the bracket pulse in the TVA servo loop, is also fed to vertical coincidence pulse transistor Q25. The purpose of the vertical coincidence circuit is to sense the instant that the tape and reference vertical sync signals occur simultaneously (coincidence), and to produce a positive-going pulse at that instant.

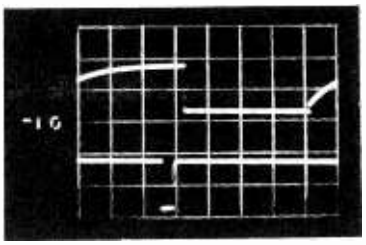
The incoming negative-going reference vertical pulse is differentiated by the network consisting of capacitor C21 and resistor R59 (see figure 39). Transistor Q24, normally saturated, is driven into cut-off by the negative-going pulse (corresponding to the leading edge of the reference vertical pulse) fed to its base. This action would normally produce a positive-going pulse at the collector of Q24; however, since vertical coincidence transistor Q25 is also normally saturated (as described below) and transistors Q24 and Q25 have a common collector circuit, there will be an output signal only when both transistors are cut off simultaneously (coincidence).

Capacitor C22 and resistor R60 form a network which differentiates the incoming tape vertical waveform. Transistor Q25, normally saturated, is driven into cut-off by the negative-going spike (corresponding to the negative-going leading edge of the tape vertical waveform) resulting from the differentiation. As mentioned in the paragraph above, transistors Q24 and Q25 must be cut off simultaneously to produce an output pulse in their common collector circuit. Thus, when the tape and reference vertical sync pulses are not properly aligned (figure 39A) there will be no output pulse (figure 39D). When the vertical pulses are aligned (figure 39B) coincidence is attained and a narrow positive-going pulse, occurring at a 60-cycle rate (50-cycle rate in International machines) appears in the common collector circuit of transistors Q24 and Q25 (figure 39C, top).

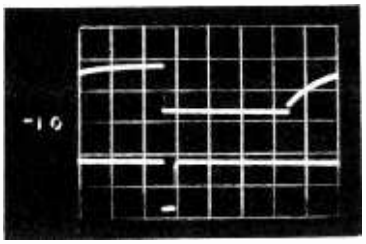
When the machine is playing back tape and tape sync is present, as detected by the sync detector circuit of the demodulator output module (no. 303), the potential on pin 12 of plug P1 is ground. The ground potential forward biases diode CR13, and when coincidence occurs the positive-going coincidence pulse is allowed to pass to the base of transistor Q26 in the lock sense circuit. In all other conditions of machine operation, the potential at pin 12 is −26 volts dc and diode CR13 is cut off. This action prevents the coincidence pulse from passing to the base of transistor Q26, and the lock sense circuit is inoperative. Therefore, there must be a video signal recorded on the tape in order to transfer control of the headwheel motor speed from the tonewheel servo to the linelock servo (pixlock). This arrangement is necessary because the operation of the linelock servo is such that in the absence of a tape sync signal, it would be possible for the headwheel motor to "run away".

Transistors Q26 and Q28 form the monostable lock sense multivibrator circuit. In the multivibrator stable state, transistor Q26 is saturated due to the base current withdrawn by the network consisting of resistor

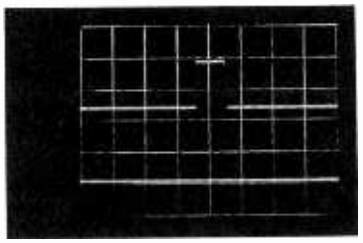




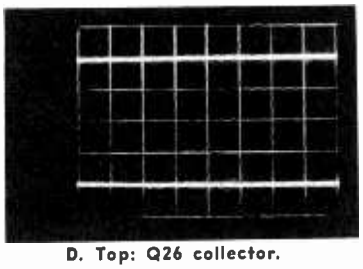
A. Top: P1-21 (TAPE VERT).
Bottom: P1-20 (REF VERT).
Non-coincidence
(2 msec/cm)



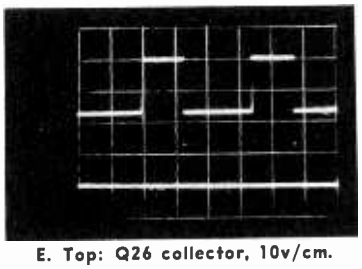
B. Top: P1-21 (TAPE VERT).
Bottom: P1-20 (REF VERT).
Coincidence
(2 msec/cm)



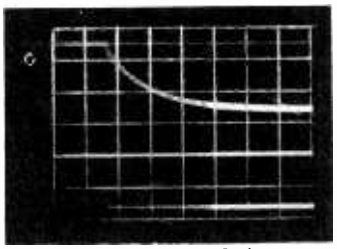
C. Top: Q25 collector.
Coincidence
Bottom: Q25 collector.
Non-coincidence
(20 μsec/cm)



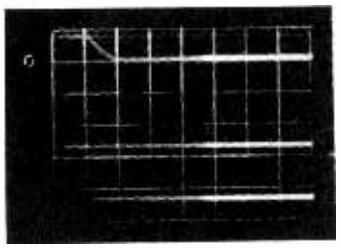
D. Top: Q26 collector.
Bottom: Q25 collector.
Non-coincidence
(5 msec/cm)



E. Top: Q26 collector, 10v/cm.
Bottom: Q25 collector.
Coincidence
(5 msec/cm)



F. Top: CR16 anode, 10v/cm.
Bottom: Q26 collector, 10v/cm.
Coincidence
(0.1 sec/cm)



G. Top: CR17 cathode.
Bottom: Q26 collector, 10v/cm.
Coincidence
(0.1 sec/cm)

Machine in PLAY mode. Servo system in PL mode when coincidence is shown and in TW mode when non-coincidence is shown. All amplitudes 5v/cm, unless otherwise noted.

Figure 39—Vertical Coincidence Pulse Generator and Lock Sense Control

R64 and diode CR14 returned to −18 volts dc, together with resistor R65 returned to ground and resistor R63 returned to +70 volts dc (figure 39D). Simultaneously, the positive potential applied to the base of transistor Q28 from the voltage divider network consisting of resistors R68 and R69 biases Q28 into cut-off. Under these conditions the collector potential of transistor Q26 is ground, and the potential across capacitor C24 is −18 volts dc with respect to the base of Q26 due to the fact that the collector of transistor Q28 is at −18 volts.

When a positive-going coincidence pulse appears at the base of transistor Q26, the transistor is driven into cut-off and its collector potential immediately falls to −18 volts (figure 39E). Transistor Q27 operates as an emitter follower, thus the potential at its emitter follows that at its base (−18 volts) and transistor Q28 is thereby driven into saturation. At the instant transistor Q28 conducts, its collector potential rises to ground. However, since the potential across capacitor C24 cannot change instantaneously, the junction of capacitor C24 and resistor R64 immediately rises to +18 volts dc. This action cuts off diode CR14, and a positive potential is applied to the base of transistor Q26 from the voltage divider network consisting of resistors R63 and R65. Transistor Q26 will then remain cut off for the duration of the timed interval; i.e., until the potential at the junction of capacitor C24 and resistor R64 goes negative once again due to C24 discharging toward −18 volts through R64. While diode CR14 is cut off, the base circuit of transistor Q26 is disconnected from the timing circuit, thereby preventing transistor and triggering circuit leakage currents from influencing the timing cycle. When capacitor C24 discharges to a negative potential whose magnitude exceeds that of the forward base-to-emitter conduction potential of transistor Q26, the transistor is driven into conduction and the timed period ends. While transistor Q26 is conducting, diode CR15 is forward biased so that capacitor C25 may discharge through Q26 to ground. Thus the reverse bias voltage on the emitter of transistor Q27 is prevented from reaching a magnitude which would cause the transistor to break down.

During tape playback in the pixlock servo mode (function selector switch on the tape sync processor module, no. 317, in PL position) and using external servo reference (SERVO REF pushbutton on PLAY panel pressed for EXT operation), the lock sense control voltage is ground. (When the SERVO REF pushbutton is pressed for EXT operation, ground is fed from 84TB1-8 to P1-18 of the tape sync processor module; when the pushbutton is pressed for LINE operation, ground is removed from P1-18 at the pushbutton switch.) In all other machine operating conditions the control voltage is −26 volts dc. This voltage is fed to the linelock module through pin 28 of plug P1 from the function selector switch in the tape sync processor module, and is applied to the emitter of linelock control transistor Q29. In the lock sense multivibrator stable state, transistor Q26 is saturated and its collector is clamped at ground potential as explained above. A potential is then established at the junction of diodes CR16 and CR17 due to the current flow from the +70 volt supply through resistors R72, R71 and diode CR16 to the emitter of transistor Q27, and through resistor R73 and diode CR17 to −18 volts. The resistance values chosen are such that the junction potential is fixed at approximately +4 volts dc, and this voltage is sufficient to hold linelock control transistor Q29 in cut-off.

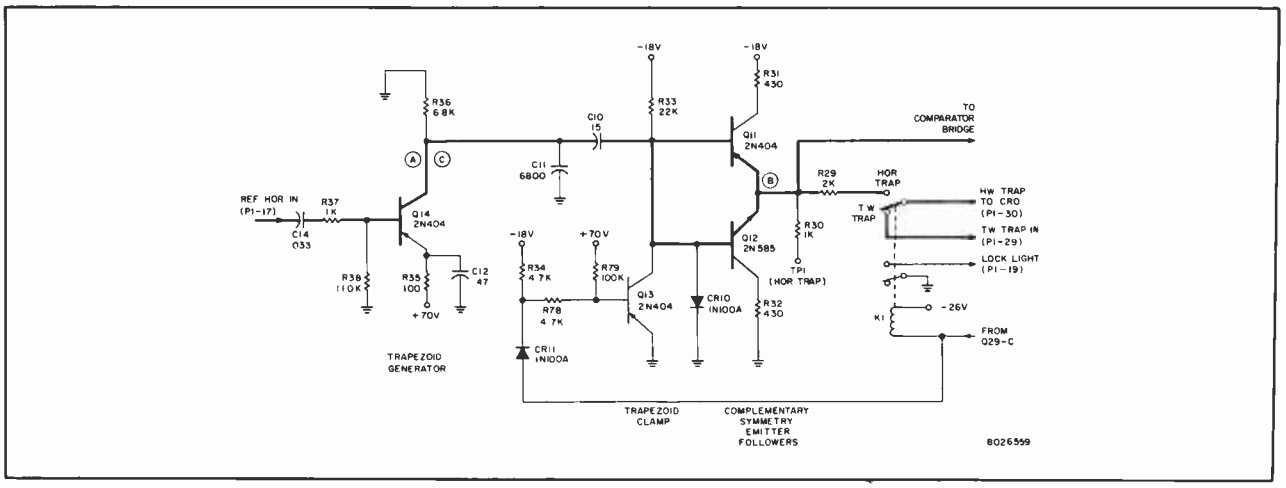
When coincidence occurs and transistor Q26 is cut off, its collector potential falls to −18 volts. Emitter follower transistor Q27 is then biased into saturation and its emitter potential follows that at its base (−18 volts). Transistor Q27 thus acts as a voltage source, providing sufficient current gain to allow the junction of diodes CR16 and CR17 to attempt to change to a new equilibrium voltage of −18 volts. However, capacitor C26 prevents the voltage from changing instantaneously since the capacitor must discharge from its fully charged state. During the interval that transistor Q26 is cut off, capacitor C26 will discharge approximately one volt. Then, as transistor Q26 is once again allowed to conduct, capacitor C26 begins to charge toward its fully charged state. When a stable state has been reached wherein coincidences occur successively on every field, the lock sense multivibrator will be triggered at a 60-cycle rate (50-cycle rate in International machines). The duty cycle of capacitor C26 is such that the discharge time of the capacitor is considerably greater than the charge time; therefore, after a number of cycles capacitor C26 will have discharged to approximately −18 volts (figure 39F).

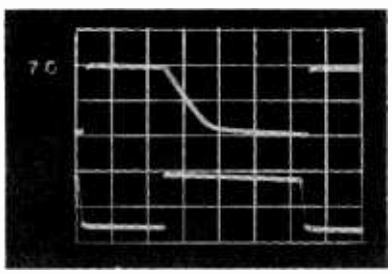
As mentioned above, the potential at the emitter of linelock control transistor Q29 is either ground or −26 volts dc, depending upon the operating conditions of the machine. When the machine is playing back tape in the pixlock servo mode with external servo reference, the emitter potential of transistor Q29 is ground. Therefore, as the voltage on capacitor C26 goes negative with respect to zero (after approximately five successive coincidence pulses), Q29 is driven into saturation and its base is clamped at zero volts (figure 39G). Diode CR17 will then be reverse-biased, thereby disconnecting transistor Q29 from the lock sense multivibrator circuit. The ground potential at the collector of transistor Q29 when the transistor is driven into conduction is the lock sense control voltage which switches control of the headwheel

motor from the tonewheel servo to the linelock servo (pixlock). Transistor Q29 will continue to conduct until a condition occurs (due to a bad tape splice or other discontinuity in the timing of the tape being played back) which causes a loss of several coincidence pulses in succession. At this point the multivibrator ceases to operate, transistor Q26 is saturated, and capacitor C26 charges back toward +4 volts dc. When the voltage on the capacitor goes positive, diode CR17 is again forward biased, and linelock control transistor Q29 is cut off, thus automatically switching the control of the headwheel motor back to the tonewheel servo.

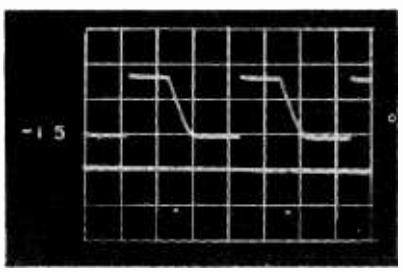
The ground potential at the collector of transistor Q29 performs two functions in the linelock module. One of the functions is to forward bias diode CR11 in the trapezoid clamping circuit of the reference horizontal trapezoid generator, thus placing the junction of resistors R34 and R78 at ground potential. The purpose of this is explained below in the *Pixlock Trapezoid Generator* discussion. A second function of the ground potential is to energize headwheel mode relay K1. When relay K1 is energized it too performs two functions. One of its functions is to supply a ground to the LOCK portion of the PIXLOCK indicator light (located above and to the left of the PLAY control panel), thus signifying that the machine is locked in the pixlock servo mode; and the other function is to feed the headwheel trapezoid waveform to the CRO monitor switcher so that it may be observed on the CRO monitor when the HW SERVO pushbutton is depressed.

In addition to the above mentioned functions of the ground potential at the collector of linelock control transistor Q29, the potential is fed through pin 3 of plug P1 to the headwheel modulator module (no. 315) where it allows the linelock error current source to determine the width of the 15 kc modulating pulse, and thus the headwheel motor speed is controlled by the linelock servo. When vertical coincidence does not occur, the linelock control transistor is cut off and the tonewheel error current source in the headwheel modulator module determines the width of the 15 kc modulating pulse. In this case the headwheel motor speed is controlled by the tonewheel servo.

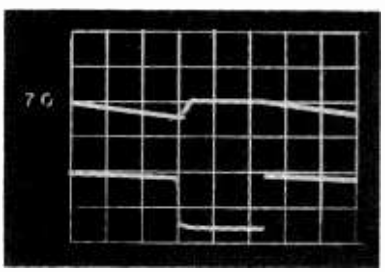




A. Top: Q14 collector.
Bottom: Q14 base.



B. Top: Q11 emitter.
Bottom: Q3 collector.
(20 μsec/cm)



C. Top: Q14 collector, 5v/cm.
Bottom: Q14 base.
STOP Mode (MOD-DEMOD)

Machine in PLAY/PL mode, sweep times 10 μsec/cm, and amplitudes 10v/cm, unless otherwise noted.

Figure 40—Pixlock Trapezoid Generator

Pixlock Trapezoid Generator

Figure 40 shows the pixlock trapezoid generator circuit, which utilizes reference horizontal sync in developing a reference trapezoid waveform when the machine is playing back tape in the pixlock servo mode with external servo reference. The trapezoid waveform is then sampled in a diode bridge circuit by a sample pulse, developed from tape horizontal sync, to produce an error signal. The pixlock trapezoid waveform is desired only when the machine is operating in the pixlock servo mode (as explained below). Therefore, in tonewheel and switchlock servo modes a clamp circuit, controlled by the lock sense control voltage, prevents formation of the trapezoid waveform.

The reference horizontal waveform, occurring at a line frequency rate, is developed in the reference generator module (no. 312) and is fed to the base of trapezoid generator transistor Q14 from pin 17 of plug P1. Transistor Q14 is normally saturated, due to the positive potential applied to its emitter. The potential at the collector of transistor Q14, and thus the voltage on capacitor C11, is then approximately +69 volts dc. When the reference horizontal signal is applied to the base of transistor Q14, the positive-going edge of the signal drives the transistor into cut-off. (See figure 41.) At the instant transistor Q14 is driven into cut-off, its collector voltage attempts to fall to ground potential; however capacitor C11, which is charged to the collector voltage of transistor Q14, cannot discharge immediately since it must discharge through resistor R36. Thus the voltage on capacitor C11, and therefore that at the collector of transistor Q14, decreases toward ground potential at a rate which is determined by the values of C11 and R36.

During the interval that transistor Q14 is saturated and the voltage on capacitor C11 is +69 volts, the common base potential of complementary symmetry emitter follower transistors Q11-Q12 is ground. Therefore, as the voltage on capacitor C11 decreases toward ground potential, the change in voltage is coupled through capacitor C10 and the base potential of transistors Q11-Q12 also decreases (i.e., increases in a negative direction from ground potential). When the negative base potential of transistors Q11-Q12 attempts to exceed −18 volts, the collector-to-base junction of transistor Q11 becomes forward biased and the base potential is clamped at −18 volts. This action prevents the voltage on capacitor C11 from decreasing further, and the voltage is thus clamped at approximately +51 volts (figure 40A). When the incoming reference horizontal waveform goes negative, transistor Q14 becomes saturated once again and its collector potential immediately rises to +69 volts. Simultaneously, capacitor C11 recharges to +69 volts and this increase in voltage is coupled through capacitor C10 to the common base circuit of transistors Q11-Q12. The potential at the bases of transistors Q11-Q12 then increases in a positive direction from −18 volts and, as the potential attempts to go positive with respect to ground, diode CR10 becomes forward biased and clamps the base potential of transistors Q11-Q12 at ground.

The reference trapezoid waveform thus formed has an amplitude of approximately 18 volts and a negative-going slope which is determined by the values of capacitor C11, resistor R36, and the +70 volt supply. Complementary symmetry emitter follower transistors Q11-Q12 lower the impedance of the trapezoidal waveform and thereby provide sufficient current gain to drive the comparator bridge circuit consisting of diodes CR4 through CR7. Test point TP1 (HOR TRAP) is provided for convenience in observing the pixlock trapezoid, which appears as shown in figure 40B.

It has been determined that the minimum time required for the headwheel motor to "lock in" at the correct speed will be obtained when the generated pixlock trapezoid waveform is first started from zero volts. Therefore, a circuit is provided which will prevent the trapezoid waveform from being formed when the machine is operating in the tonewheel or switchlock servo modes, and will thus cause the waveform to begin from the zero voltage reference when the machine attains a "lock" in the pixlock servo mode. Trapezoid clamp transistor Q13 and associated circuit components perform this function in the following manner:

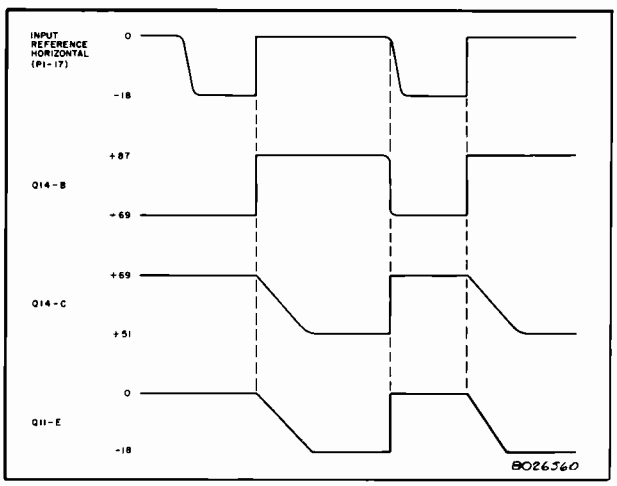


Figure 41—Pixlock Trapezoid Waveforms

During tape playback in the pixlock servo mode with external servo reference, a ground potential from the collector of linelock control transistor Q29 in the lock sense circuit forward biases diode CR11. The junction of resistors R34 and R78 is then clamped at ground potential, thus causing a positive bias voltage to be applied to the base of trapezoid clamping transistor Q13 from the voltage divider network consisting of resistors R78 and R79 returned to +70 volts. The positive bias voltage holds transistor Q13 in cut-off, thus allowing the trapezoid generator circuit to function as described above. When the machine is operated in tonewheel or switchlock servo mode, diode CR11 is reverse-biased by −26 volts dc on its anode. In this case current is withdrawn from the base of transistor Q13, due to the action of the network consisting of resistors R34, R78, and R79. The base current biases transistor Q13 into saturation, and this prevents the potential at the bases of complementary symmetry emitter follower transistors Q11-Q12 from going negative. Thus the pixlock trapezoid waveform will not be developed, and the waveform at the collector of trapezoid generator transistor Q14 appears as shown in figure 40C.

The lock sense control voltage which establishes the bias potential on diode CR11 also determines the state of headwheel mode relay K1. During tape playback in the pixlock servo mode with external servo reference, the ground potential at the collector of linelock control transistor Q29 is fed to the coil of relay K1. This causes the relay to become energized and thus allow the generated pixlock trapezoid waveform to be fed through pin 30 of plug P1 to the CRO monitor switcher. The pixlock trapezoid waveform may then be observed on the CRO monitor by pressing the HW SERVO pushbutton. (When the machine is operated in any manner other than tape playback in the pixlock servo mode with external servo reference, relay K1 is deenergized. This allows the tonewheel trapezoid waveform, generated in the tonewheel servo module, to be fed to the CRO monitor switcher so that it may be observed on the CRO monitor when the HW SERVO pushbutton is depressed.)

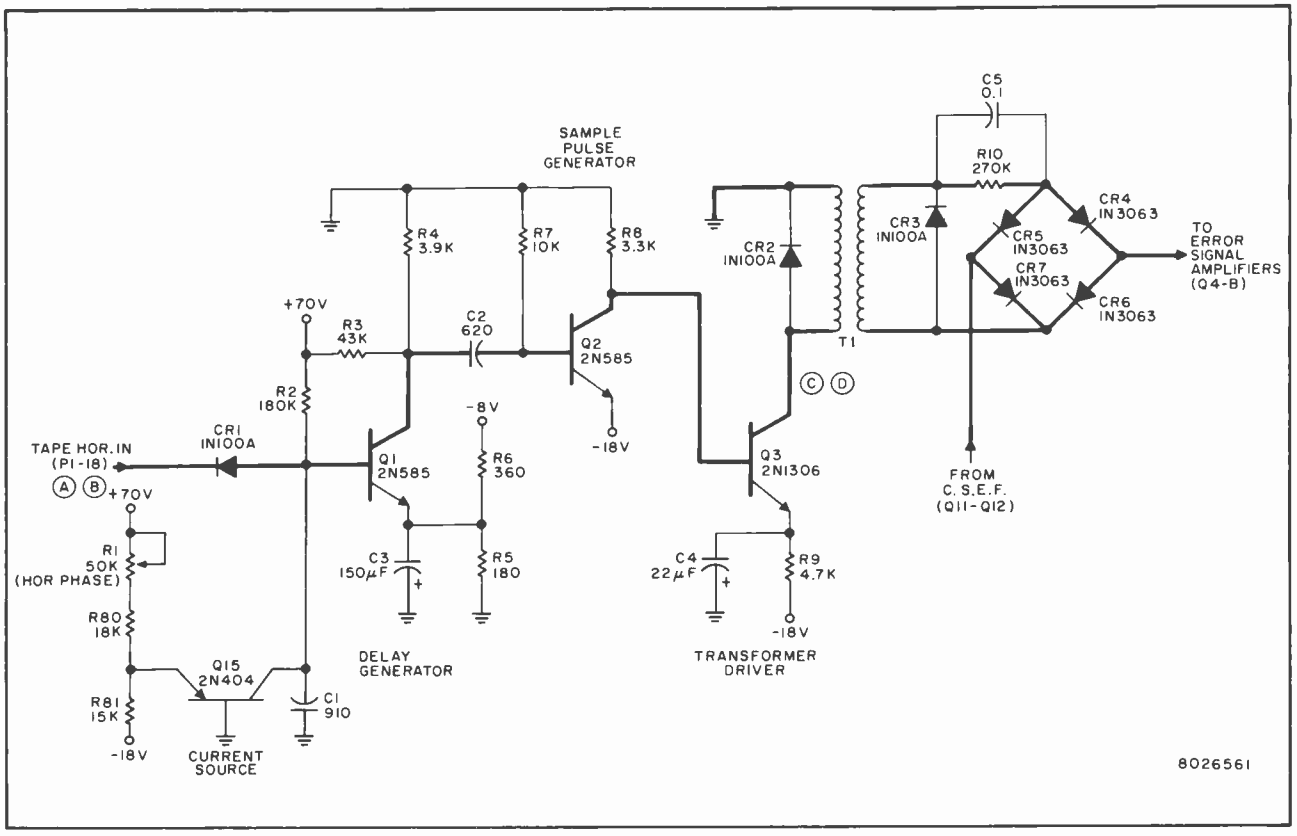
Tape Horizontal Delay and Sample Pulse Generator

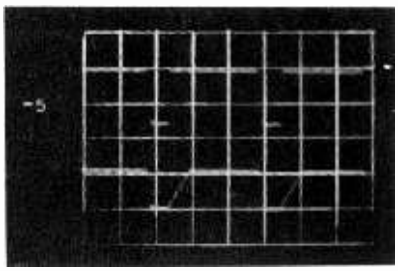
The tape horizontal delay and sample pulse generator circuits (figure 42) utilize tape horizontal sync in developing a pulse which samples the pixlock trapezoid waveform in a comparator bridge circuit. An adjustable delay network is provided in the sample pulse circuitry so that the half-slope delay, explained above in the *TVA Servo* discussion, may be obtained.

The tape horizontal waveform enters the module through pin 18 of plug P1 from the tape sync processor module (no. 317), and is shown in figures 42A and 42B. The waveform, occurring at a line frequency rate, is then fed to the delay generator circuit consisting of transistors Q1 and Q15, and associated circuit components. During the negative portion of the incoming tape horizontal waveform, the magnitude of the voltage at pin 18 of plug P1 will lie between the approximate limits of −6.75 and −8 volts dc, depending upon the setting of potentiometer R1 (as explained below). The negative voltage forward biases diode CR1, and thus the voltage appears at the base of delay generator transistor Q1 and across capacitor C1. Since the bias potential applied to the emitter of transistor Q1 is approximately −2.6 volts dc, due to the action of the voltage divider network consisting of resistors R5 and R6, the transistor is cut off. When transistor Q1 is cut off, the voltage divider network consisting of resistors R3 and R4 establishes a potential of approximately +8 volts dc at its collector.

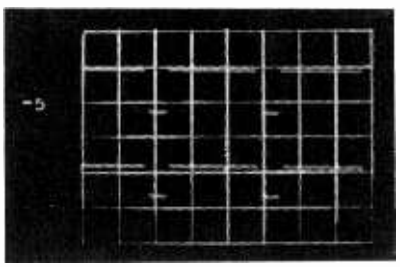
The positive-going edge of the incoming tape horizontal waveform, rising sharply to ground potential, reverse-biases diode CR1 and thus disconnects the input circuit from the delay generator circuit. Capacitor C1 then begins to discharge through resistor R2 at a rate which is determined by the value of R2 returned to +70 volts, and by the magnitude of the current supplied by current source transistor Q15. When the voltage on capacitor C1 reaches −2.6 volts, transistor Q1 is driven into saturation and its base is clamped at −2.6 volts. The voltage at the collector of transistor Q1 then falls rapidly to approximately −2.6 volts, and remains at this level until the incoming tape horizontal waveform goes negative once again and causes the transistor to be cut off.

Current source transistor Q15 operates as a common base amplifier, and the degree to which it conducts depends upon the current supplied to its emitter. This current in turn is determined by the setting of potentiometer R1 (HOR PHASE control). The values of resistors R80, R81, and potentiometer R1, in the emitter biasing network of transistor Q15, are such that the transistor is cut off when R1 is rotated fully counterclockwise (maximum resistance). In this condition there will be no current supplied by transistor Q15, thus the negative level of the incoming tape horizontal waveform will be approximately −8 volts and capacitor C1 will discharge at a comparatively slow rate (figure 42A). When potentiometer R1 is rotated fully clockwise (minimum resistance), transistor Q15 is biased so that it will supply approximately 2.7 milliamperes of current to the discharge circuit of capacitor C1 and will thus increase the rate at which the capacitor discharges (figure 42B). In

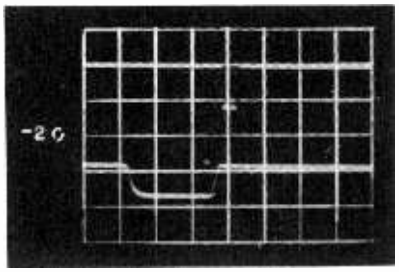




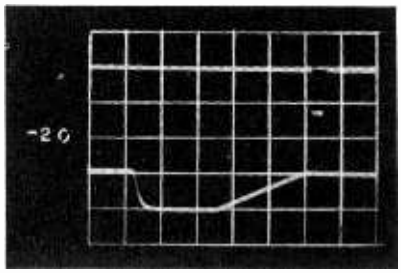
A. Top: P1-18 (TAPE HOR). Bottom: Q1 base. Maximum Delay (20 μsec/cm)



B. Top: P1-18 (TAPE HOR). Bottom: Q1 base. Minimum Delay (20 μsec/cm)



C. Top: Q3 collector, 10v/cm. Bottom: Q1 base. Minimum Delay (5 μsec/cm)



D. Top: Q3 collector, 10v/cm. Bottom: Q1 base. Maximum Delay (5 μsec/cm)

Machine in STOP mode (MOD-DEMOD). All amplitudes 5v/cm, unless otherwise noted.

Figure 42—Tape Horizontal Delay and Sample Pulse Generator

addition, when transistor Q15 is supplying 2.7 milliamperes of current the negative level of the incoming tape horizontal waveform is approximately −6.75 volts due to a potential drop across the collector resistor of horizontal output transistor Q5 in the tape sync processor module.

Therefore, since capacitor C1 cannot discharge immediately to the −2.6 volt potential which will cause delay generator transistor Q1 to saturate, a delay is generated between the time at which the tape horizontal waveform goes positive and the time at which transistor Q1 saturates. This delay (the half-slope delay) is adjustable between the approximate limits of 2 microseconds and 12 microseconds by rotating the HOR PHASE control (potentiometer R1). Thus a positive-going pulse is produced at the collector of transistor Q1 whose negative-going edge is delayed with respect to the positive-going edge (timed to tape horizontal sync) of the incoming tape horizontal waveform, by an interval which is dependent upon the setting of the HOR PHASE control. (The proper procedure for obtaining the correct control setting is outlined under *Adjustments.*)

The positive-going pulse at the collector of transistor Q1 is differentiated by the network consisting of capacitor C2 and resistor R7, and the differentiated signal is fed to the base of sample pulse generator transistor Q2 in a pulse-narrowing boxcar circuit. Transistor Q2, normally biased into saturation, is driven into cut-off by the negative-going spike resulting from the differentiation. When transistor Q2 is driven into cut-off, its collector potential immediately rises toward ground until it reaches a level which allows transformer driver transistor Q3, normally biased at cut-off, to conduct. As transistor Q3 conducts, it clamps the collector of transistor Q2 at this level for an interval which is determined by the values of resistor R7 and capacitor C2. The actual level at which the collector of transistor Q2 will be clamped depends upon the bias voltage developed at the emitter of transistor Q3. This voltage in turn is determined by the repetition rate (which is dependent upon the line standard used) and the pulse duration of the output from transistor Q2, as well as by the current required by pulse transformer T1.

The resulting output at the collector of transistor Q3 (figures 42C and 42D), is a narrow, negative-going sample pulse whose width is determined by the values of resistor R7 and capacitor C2 in the boxcar circuit of transistor Q2. (Figure 42C shows the sample pulse when the HOR PHASE control is rotated to obtain minimum delay, while figure 42D shows the pulse with the control rotated to obtain maximum delay.) Transistor Q3 provides the current gain required to drive pulse transformer T1, and diode CR2 is inserted into the collector circuit of Q3 to suppress the inductive kick-back of the transformer.

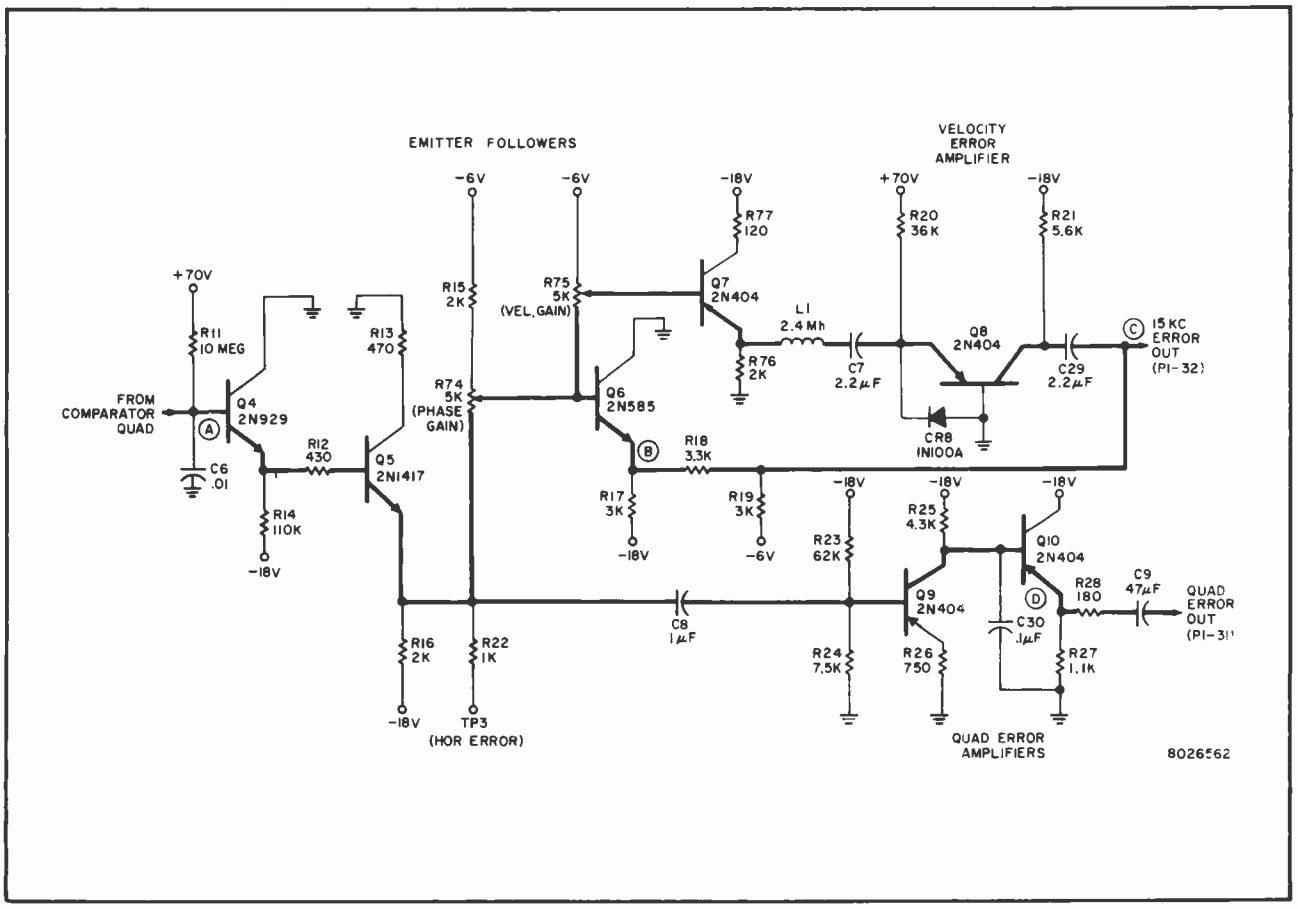
Pulse transformer T1 splits the sample pulse phase and drives opposite ends of the diode bridge consisting of diodes CR4 through CR7, as shown in figure 42. The diode bridge is also driven by the pixlock trapezoid waveform which is developed as explained above in the *Pixlock Trapezoid Generator* discussion. During the sample pulse interval the diodes of the bridge are forward biased, thus providing a low impedance path between storage capacitor C6 and complementary symmetry emitter follower transistors Q11-Q12. Capacitor C6 then charges to the potential of that portion of the trapezoid which occurs during the pulse interval. The capacitor maintains this potential during the interval between sample pulses, when the diodes of the comparator bridge are cut off and the capacitor becomes disconnected from the complementary symmetry emitter follower transistors.

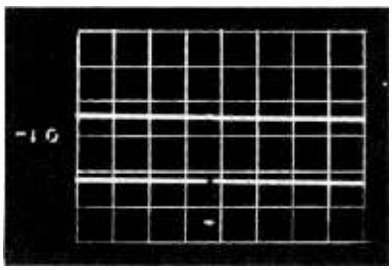
In the pixlock servo mode, if the headwheel motor is running at a constant speed with tape horizontal sync aligned with reference horizontal sync, the sample pulse will sample very near the center of the trapezoid slope, due to the half-slope delay introduced by the delay generator circuit. If the headwheel motor accelerates or decelerates slightly, the sample pulse will move up or down on the trapezoid slope. As the sample pulse moves up on the slope (i.e., toward ground potential), transistor Q11 becomes biased at cut-off and transistor Q12 is biased into conduction. Capacitor C6 will then discharge toward ground through transistor Q12. Conversely, as the sample pulse moves down on the slope (i.e., toward −18 volts), transistor Q12 is biased at cut-off and transistor Q11 is biased into conduction. In this case, capacitor C6 charges toward −18 volts through transistor Q11.

The voltage on capacitor C6 is thus a function of the headwheel motor speed, and any deviation of the sample pulse from the center reference of the trapezoid slope will generate a d-c signal. This signal is the 15 kc error signal, which is fed to the headwheel modulator module following current amplification as described in the *Error Signal Amplifier* description below.

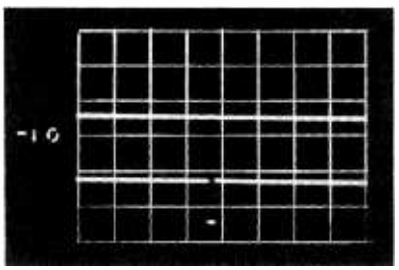
Error Signal Amplifiers

The d-c error signal developed from the comparison of waveforms derived from tape horizontal sync and reference horizontal sync in the comparator bridge circuit is fed to emitter follower transistors Q4 and Q5 in series (figure 43A). Transistors Q4 and Q5 act as current gain transistors, and the d-c error signal

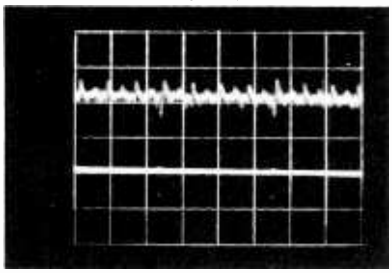




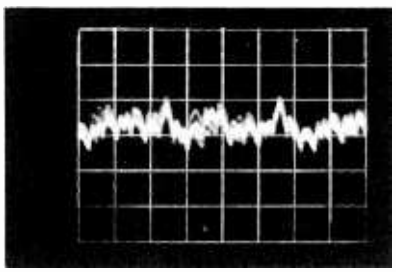
A. Top: Q4 base, 5v/cm.
Bottom: Q3 collector.
(10 μsec/cm)



B. Top: Q6 emitter, 5v/cm.
Bottom: Q3 collector.
(10 μsec/cm)



C. Top: P1-32 (15 KC ERR), 1v/cm.
Bottom: Q17 collector.
(5 msec/cm)



D. Q10 emitter, 1v/cm.
(5 msec/cm)

Machine in PLAY/PL mode. All amplitudes 10v/cm, unless otherwise noted.

Figure 43—Error Signal Amplifiers

output at the emitter of Q5 may be observed at test point TP3 (HOR ERROR). The error signal is fed from the emitter of transistor Q5 to potentiometer R74 (PHASE GAIN), and also to the quad error amplifier circuit which is explained below.

Potentiometer R74 controls the magnitude of the d-c error signal which is fed to emitter follower transistor Q6 and, through potentiometer R75 (VEL GAIN), to emitter follower transistor Q7. Additional current gain is provided by transistor Q6, and the error signal at its emitter (figure 43B) is an indication of the difference in frequency between the tape and reference horizontal sync signals. Since this frequency difference is generally less than one cycle, the error signal is d-c and is referred to as the *phase* error signal. The phase error signal is then fed to pin 32 of plug P1, where it is combined with the velocity error signal obtained from the velocity error amplifier circuit.

The magnitude of the d-c error signal fed to the base of emitter follower transistor Q7 in the velocity error amplifier circuit is dependent upon the setting of potentiometer R74, and is further controlled by potentiometer R75. (The correct procedure for adjusting potentiometers R74 and R75 is explained under *Adjustments*.) Transistor Q7 amplifies the error signal current, and the signal at the emitter of Q7 is fed to a differentiating network consisting of capacitor C7 and the low emitter impedance of common base amplifier transistor Q8. Since the error signal fed to the differentiating network is d-c, only *changes* in error signal magnitude (corresponding to headwheel velocity errors) will be amplified by transistor Q8. Diode CR8 provides a discharge path for capacitor C7 whenever a very large, sudden change in error signal occurs in such a direction as to cut off transistor Q8. In addition to forming part of the differentiating network, capacitor C7 in series with coil L1 forms a low-pass filter network whose purpose is to reduce the magnitude of the transients resulting from sampling. This is desirable because transistor Q8 provides a very high voltage gain, and the large sampling transients would be amplified to such a level as to cause the modulator to overload.

The velocity error signal is amplified by transistor Q8 and fed to pin 32 of plug P1, where it is combined with the d-c phase error signal (figure 43C). The combined error signal is fed from pin 32 to the headwheel modulator module (no. 315) where it controls the linelock error current source transistor when the machine is locked in the pixlock servo mode.

The error signal at the emitter of emitter follower transistor Q5 is also fed to the quad error amplifier circuit, as mentioned above. This circuit functions in a manner similar to the velocity error amplifier circuit, in that error signal *changes* are amplified, and the purpose of the circuit is to provide a signal which may be a-c coupled to the CRO monitor for presentation on the monitor.

Capacitor C8 and resistors R23 and R24 form a differentiation network which suppresses the very low frequency error signal components. Transistor Q9 amplifies the remaining signal, and the integrating network consisting of capacitor C30 and resistor R25 acts as a low-pass filter in removing the higher frequency components of the error signal. Thus the resulting error signal contains a narrow band of frequencies which approximates that of the output from the velocity amplifier circuit. The error signal (figure 43D) is fed through pin 31 of plug P1 to the CRO monitor switcher, and may be observed on the CRO monitor during pixlock servo operation by pressing the QUAD ADJ pushbutton on the switcher.

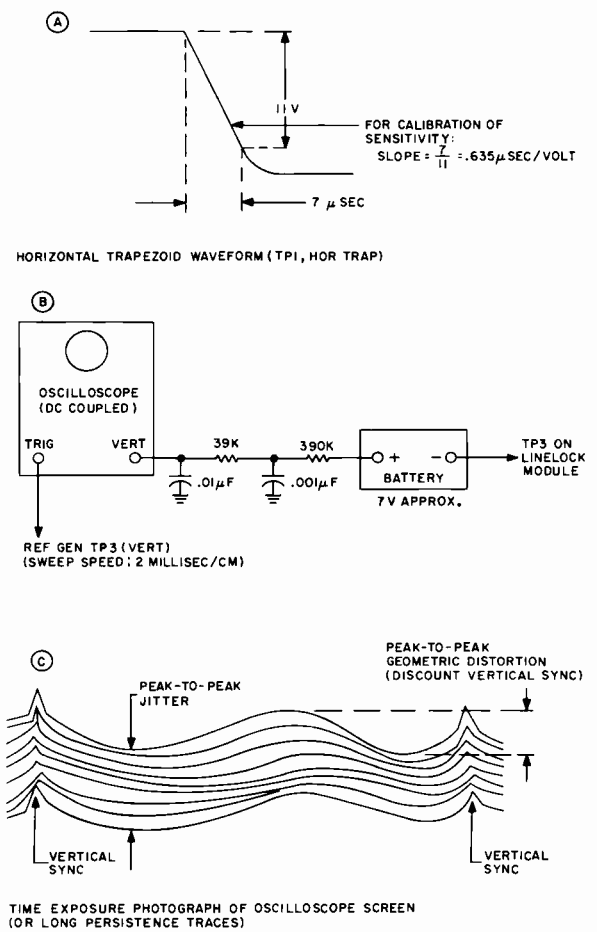


Figure 44—Measurement of Jitter and Geometric Distortion

Adjustments

Horizontal Phase Control

The horizontal phase control (HOR PHASE) permits phasing the picture horizontally so that the tape and external signals coincide. A procedure for properly adjusting the control is as follows:

1. Play back a tape in the pixlock servo mode (function selector switch on the tape sync processor module, no. 317, in PL position).

2. Operate the CRO monitor on external sync (EXT SYNC), and press the H and EXP pushbuttons (to the right of the CRO monitor).

3. Press the VID IN and VID OUT pushbuttons on the CRO monitor switcher simultaneously, so that the video input and video output signals are superimposed on the CRO monitor.

4. Rotate the HOR PHASE control to obtain coincidence between the timed edge of the horizontal sync on the input and output video signals.

NOTE: A similar procedure may be followed at the station or studio output switcher.

Phase and Velocity Gain

The gain of both the phase loop and the velocity loop of the linelock servo is controlled by the PHASE GAIN screwdriver adjustment, while the VEL GAIN screwdriver adjustment provides a separate means of adjusting the velocity loop gain. As these gains are increased, the result is an increasingly greater geometric distortion of the picture, rather than a clear oscillation. Test equipment required includes the *Tektronix Type 535-A* oscilloscope or the equivalent.

1. Rotate the VEL GAIN and PHASE GAIN screwdriver adjustments fully clockwise.

2. Rotate the HEAD SELECT switch on the Reference Generator module (no. 312) to no. 1 position.

3. Play back a tape with the machine operating in the switchlock (SL) servo mode, and adjust the C. T. PHASE control (on the PLAY control panel) so that head no. 1 is playing back vertical sync.

4. Rotate the function selector switch on the tape sync processor module (no. 317) to PL position.

NOTE: If the machine has not been completely aligned, it should be done at this time. Emphasis should be placed on channel equalization, the removal of jogs and scallops, etc. to obtain the best possible picture.

5. Rotate the PHASE GAIN adjustment to the center of its range.

6. Press DEMOD OUT on the picture monitor switcher and rotate the VEL GAIN adjustment in the counterclockwise direction until the servo system begins to oscillate. Note this point.

7. Rotate the VEL GAIN adjustment in the clockwise direction until excessive geometric distortion occurs. Note this point.

8. Set the VEL GAIN adjustment approximately midway between the points noted in steps 6 and 7. (The final setting of the VEL GAIN adjustment should be at least 15 degrees of shaft rotation in a clockwise direction from the point of oscillation.)

9. If satisfactory results are not obtained, readjust the PHASE GAIN adjustment in the desired direction as indicated by the response of the system to a gradual increase in load on the headwheel motor. Readjust the VEL GAIN adjustment as described in steps 6, 7, and 8 above.

10. After the above steps have been completed, proper operation of the linelock servo may be checked in the following manner:

a. With the machine in the PLAY mode, place the oscilloscope probe on the HOR TRAP test point and measure the amplitude of the negative-going trapezoid slope, beginning at the leading edge of the slope as shown in the example (figure 44A). In the example, the amplitude "a" is assigned an arbitrary value of 11 volts. Therefore:

$$\frac{t}{a} = \frac{7}{11} = .635 \text{ microseconds/volt}$$

The specified maximum jitter is ± 0.1 microsecond for ball-bearing headwheel panels, and ± 0.07 microsecond for air-bearing headwheel panels. Therefore:

$$\pm \frac{.1}{.635} = \pm .157 \text{ volt peak (.31 volts peak-to-peak)}$$

in the example shown. In practice this figure will vary with the steepness of the slope.

b. To measure the horizontal error signal, connect the oscilloscope probe to the HOR ERROR test point through a 500 cps low-pass filter and battery as shown in figure 44B. The filter removes the 15 kc component of the error signal, but allows the lower frequency jitter and distortion components of the signal to appear on the oscilloscope as shown in figure 44C. Measurement of geometric distortion and peak-to-peak jitter may then be made directly on the oscilloscope.

NOTE: Jitter is specified as the peak-to-peak excursion of the error signal as observed over an interval of 30 seconds. To measure the jitter, carefully observe the peak up and down excursion of the error signal on the oscilloscope during a 30 second interval; or, to obtain greater accuracy, make a 30 second time exposure of the waveform presentation on the oscilloscope and measure the thickness of the resulting trace (see figure 44C).

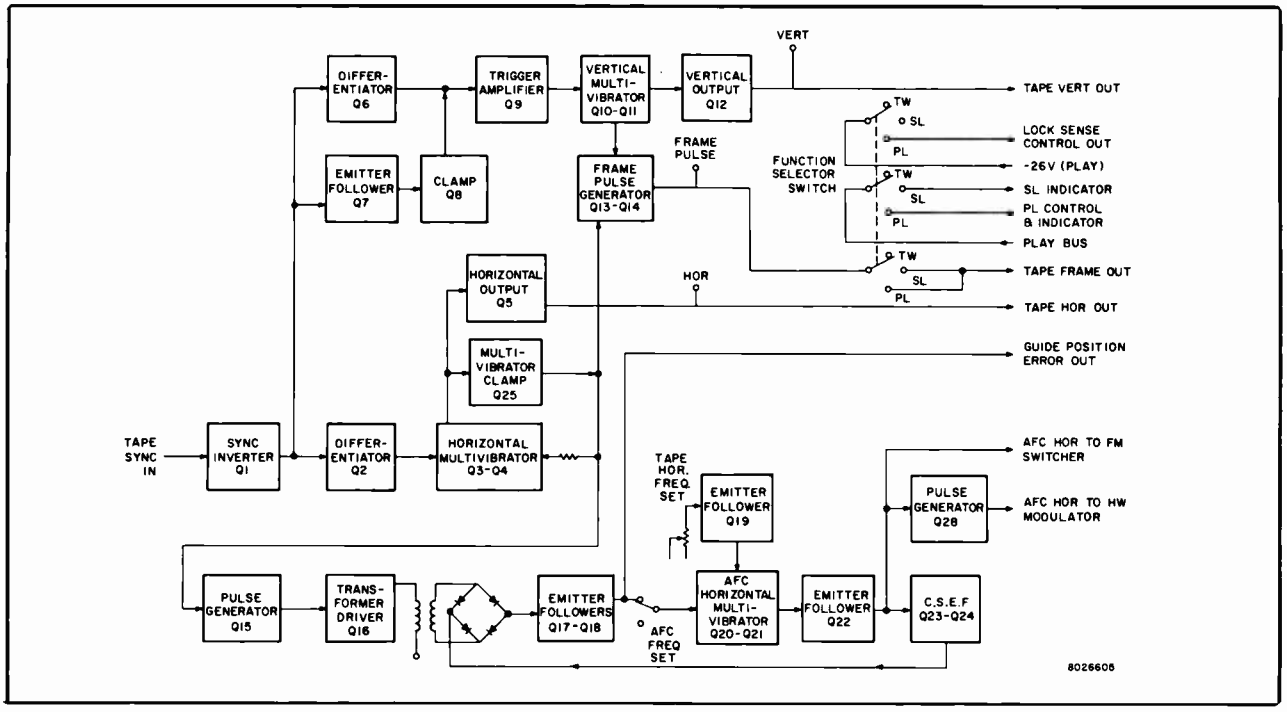


Figure 45—Tape Sync Processor Module Block Diagram

TAPE SYNC PROCESSOR (DOMESTIC)

Circuit Description

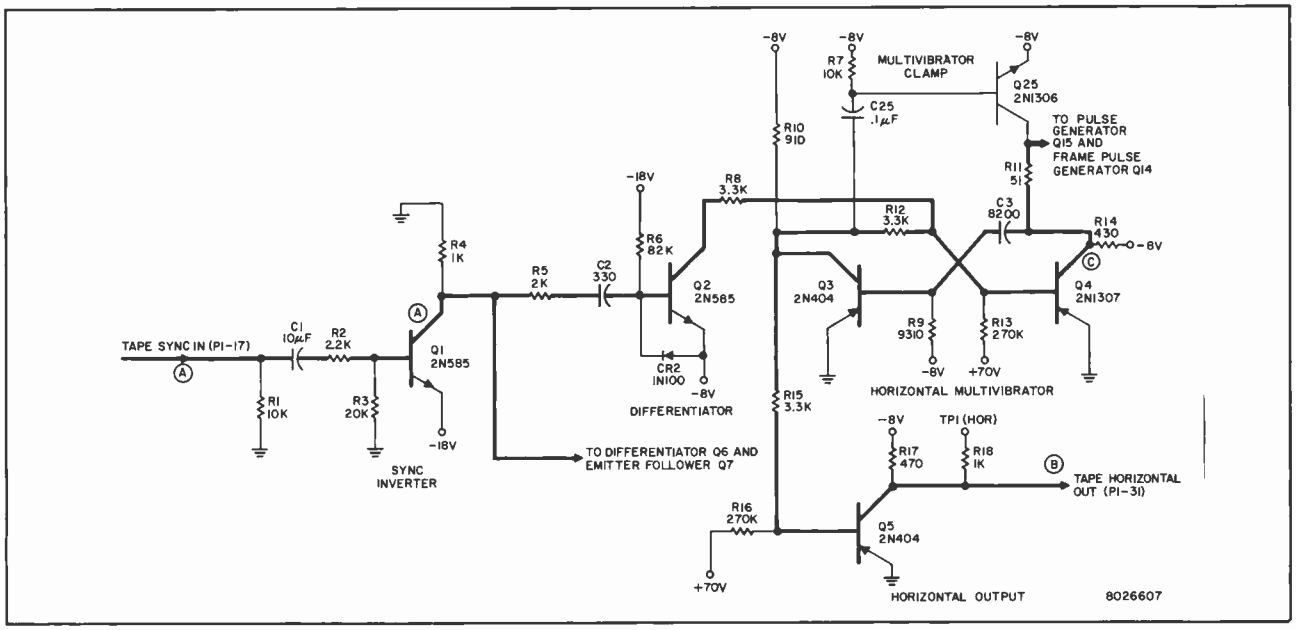
General

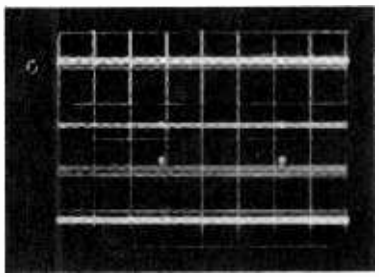
The function of the tape sync processor module (no. 317) is to utilize stripped tape sync, obtained during tape playback from the demodulator output module (no. 303), in deriving (1) horizontal sync; (2) vertical sync; (3) a tape frame pulse; (4) an advanced horizontal sync pulse at the average tape sync frequency; and (5) the 960-cycle frequency modulation component contained in the tape sync. (The tape sync processor module also derives horizontal and vertical sync signals from sync stripped from the video signal obtained in other machine modes during back-to-back, or MOD-DEMOD, operation.) The horizontal and vertical sync signals are taken directly from composite tape sync and are utilized in generating the tape frame pulse. The advanced horizontal sync pulse is obtained from a trapezoid-type horizontal frequency afc circuit which utilizes the separated horizontal sync as a reference; and the 960-cycle frequency modulation component is taken directly from the error signal within the afc loop.

Separated vertical sync, in addition to its function in the development of the tape frame pulse, is fed to the linelock module (no. 316) where it is formed into the "bracket" sampling pulse in the tape vertical alignment (TVA) servo loop and is compared in phase with reference vertical sync in a coincidence circuit which governs the development of the lock sense control voltage. Separated horizontal sync, in addition to its function in the afc loop and in the development of the tape frame pulse, is also fed to the linelock module, where it is compared with reference horizontal sync to develop an error signal during linelock (pixlock) servo control of the headwheel motor speed.

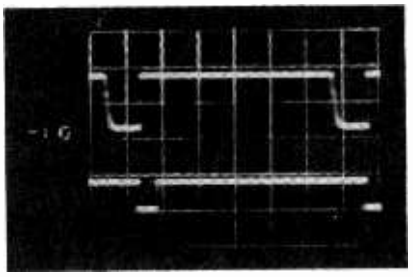
The horizontal afc loop serves three purposes essential to optimum operation of the machine during tape playback. They are (1) to provide the FM switcher module (no. 318) with a waveform having an edge which is advanced so that video head switching will take place during the first horizontal sync pulse interval which occurs in the head "overlap" region; (2) to provide an error signal which is utilized by circuitry in the guide servo module (no. 221) in positioning the vacuum guide to remove "jogs" along the vertical edges of the picture during automatic guide operation; and (3) to provide a pulse at the horizontal rate which is fed to the headwheel modulator module where it is utilized as the modulating pulse in controlling the headwheel motor speed.

In addition to the various circuits mentioned above, the tape sync processor module contains the three-position servo mode selector switch. This switch controls particular circuits which are utilized by the machine according to whether the servo system is operated in tonewheel (TW) switchlock (SL), or pixlock (PL) servo mode. (See block diagram, figure 45.)

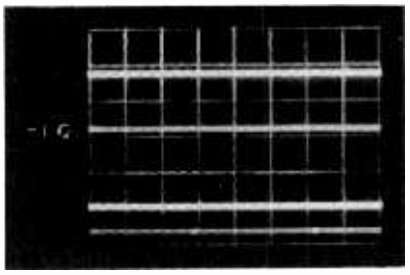




A. Top: P1-17 (TAPE SYNC). Bottom: Q1 collector, 10v/cm.



B. Top: Q5 collector, 5v/cm. Bottom: P1-17 (TAPE SYNC). (10 μsec/cm)



C. Top: Q4 collector, 5v/cm. Bottom: P1-17 (TAPE SYNC).

Machine in STOP mode (MOD-DEMOD). All sweep times 5 msec/cm, and amplitudes 2v/cm, unless otherwise noted.

Figure 46—Tape Horizontal Sync Pulse Generator

Tape Horizontal Sync Pulse Separator

The tape sync signal, containing horizontal and vertical sync, is fed from the demodulator output module (no. 303) through pin 17 of plug P1 to the base of sync inverter transistor Q1 (figure 46A). Transistor Q1 is normally biased into conduction, and its collector potential is then −18 volts dc. When a negative-going sync pulse appears at its base, transistor Q1 is driven into cut-off and its collector potential rises to approximately ground. Thus the incoming tape sync signal is inverted and amplified, as shown in figure 46A.

The signal at the collector of transistor Q1 is fed simultaneously to differentiator transistor Q2 and to differentiator transistor Q6 and emitter follower transistor Q7 in the tape vertical sync pulse separator circuit. Capacitor C2 and resistor R6 form a network which differentiates the output signal from transistor Q1, and the differentiated signal is then fed to the base of transistor Q2. Differentiator transistor Q2 is normally cut off, and its collector potential is then ground. The positive-going edge of the differentiated signal fed to the base of Q2 drives the transistor into conduction, and the signal at the collector of Q2 is fed to the base of transistor Q4. Diode CR2 furnishes a discharge path for capacitor C2 and also insures that transistor Q2 is held in cut-off during the interval between sync pulses by a reverse-bias voltage equal to the contact potential of the diode.

Transistor Q4 combines with transistor Q3 to form the monostable horizontal multivibrator. In the multivibrator stable state, transistor Q3 is biased into conduction by the current withdrawn from its base through resistor R9 returned to −8 volts. Simultaneously, transistor Q4 is biased at cut-off by the positive potential applied to its base from the voltage divider network consisting of resistor R13 returned to +70 volts and resistor R12 returned to the ground poten-

tial at the collector of transistor Q3 when Q3 is conducting. When differentiator transistor Q2 is driven into conduction, its collector potential decreases from ground to −8 volts. This voltage develops a current, limited by resistor R8, which is fed to the base of transistor Q4 and thereby drives Q4 into conduction. However, during the interval that transistor Q4 is cut off, the potential at its collector is −8 volts and the base of transistor Q3 is at ground potential; therefore capacitor C3 is charged to −8 volts. At the instant transistor Q4 begins to conduct, its collector voltage rises very rapidly to ground potential and the full charge across capacitor C3 is applied to the base of transistor Q3. The charge across capacitor C3 is then +8 volts with respect to the base of transistor Q3, thus Q3 is cut off.

This action begins the one-shot period of the multivibrator, and the duration of the period is determined by the discharge rate of capacitor C3 through resistor R9 toward −8 volts. When the voltage at the base of transistor Q3 goes negative, Q3 is driven into conduction once again and the timed period ends. The timed period exceeds that of half a TV line so that the multivibrator divides by two during the double rate pulses in the 9H interval of vertical blanking. Thus, the horizontal multivibrator removes all vertical components and produces a waveform occurring at the horizontal rate.

Because the signal at the collector of transistor Q4 is fed into a relatively large capacitive load, the d-c potential at its collector would not normally fall rapidly to −8 volts when transistor Q4 is driven into cut-off (at the end of the timed period). This condition is undesirable because any spurious signal occurring while the collector potential of transistor Q4 is falling toward −8 volts will act as a false multivibrator triggering pulse. To eliminate accidental triggering, especially during the vertical sync interval, the multivibrator clamp circuit consisting of transistor Q25 and associated circuit components is utilized. When transistor Q3 is driven into conduction, the positive-going edge of the voltage transition at its collector drives transistor Q25 into conduction. This action effectively places resistor R11 in parallel with resistor R14, and the resulting time constant (R11-R14 in conjunction with the load capacitance) is shortened by a ratio of approximately 10 to 1. Thus the potential at the collector of transistor Q4 will fall to −8 volts very rapidly, thereby resulting in a very high multivibrator duty cycle (approximately 80%). The high duty cycle insures that the multivibrator can be re-triggered only during the final 20% of a TV line, and therefore immunity to noise and other spurious pulses is attained.

The signal at the collector of transistor Q3 is fed to the base of horizontal output transistor Q5 which isolates the multivibrator from the output load. The tape horizontal signal, shown in figure 46B, is fed from pin 31 of plug P1 to the linelock module (no. 316) and may be observed at test point TP1 (HOR). The output signal at the collector of transistor Q4 (figure 46C) is used in two separate pulse generating circuits which will be described later.

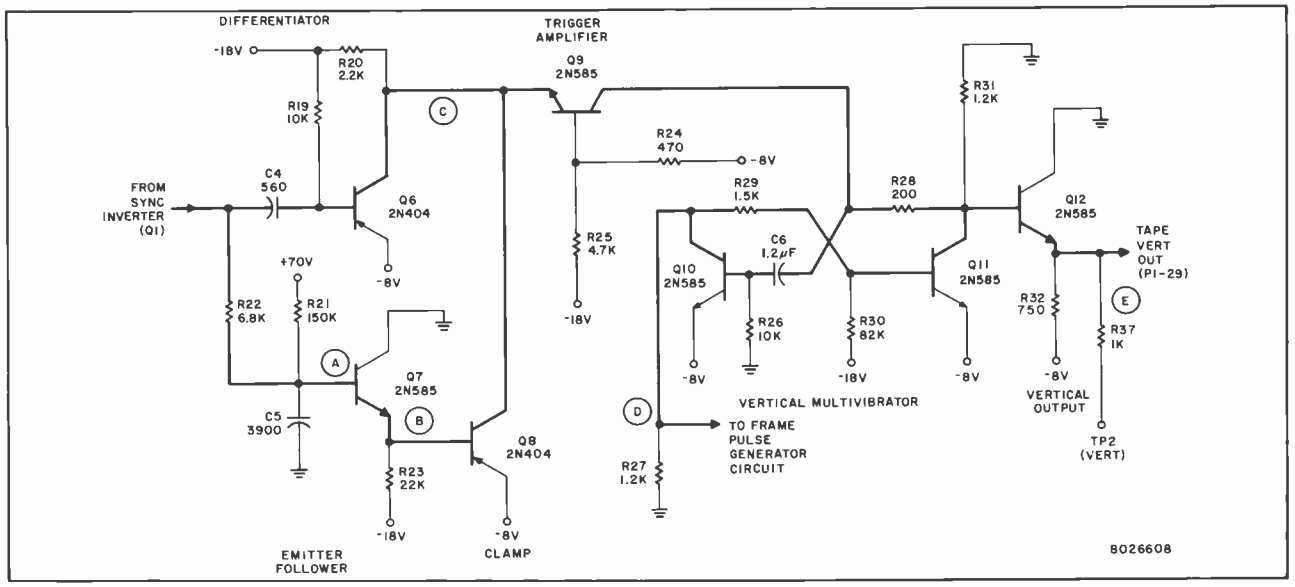
Tape Vertical Sync Pulse Separator

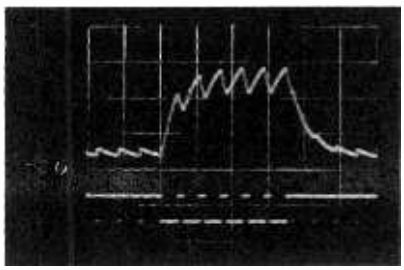
As mentioned previously, the tape sync signal at the collector of sync inverter transistor Q1 is fed simultaneously to differentiator transistor Q6 and to emitter follower transistor Q7 in the tape vertical sync pulse separator circuit. Differentiator transistor Q6 functions in the familiar manner of the pulse narrowing boxcar circuit. The transistor is biased into conduction by the current withdrawn from its base through resistor R19 returned to −18 volts, and its collector potential is then driven to −8 volts. When a positive-going pulse from the collector of transistor Q1 is applied to the base of transistor Q6 through capacitor C4, Q6 will be cut off for an interval which is proportional to the time constant determined by the values of capacitor C4 and resistor R19.

During the interval that differentiator transistor Q6 is cut off, its collector voltage attempts to fall to −18 volts. However, it is prevented from doing so because it is clamped at −8 volts by clamping transistor Q8, which is normally saturated by the current withdrawn from its base through resistor R23 returned to −18 volts. Therefore, no signal can appear at the collector of transistor Q6 until the clamping action of transistor Q8 is removed.

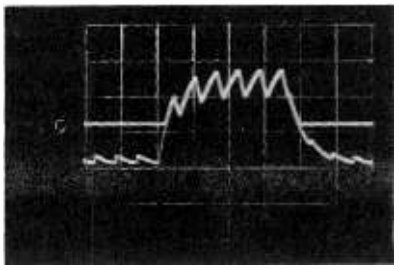
In addition to driving differentiator transistor Q6, the signal at the collector of sync inverter transistor Q1 is integrated by the network consisting of resistor R22 and capacitor C5, and is then applied to the base of emitter follower transistor Q7 (figure 47A). The time constant of the integrator network is such that the output charges to approximately 80% of its maximum amplitude within a period equal to that of one half a TV line. Thus the amplitude of the integrator network output is low when horizontal sync appears, and high when vertical sync appears.

Transistor Q7 is biased at cut-off by the voltage applied to its base through resistor R21 in conjunction with the output from transistor Q1 fed through resistor R22. When the positive-going output from the integrator network exceeds the negative cut-off bias voltage of transistor Q7, it causes Q7 to conduct. The integrated signal then appears at the emitter of transistor Q7, as shown in figure 47B. In figure 47B, the

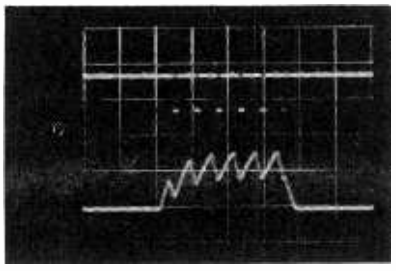




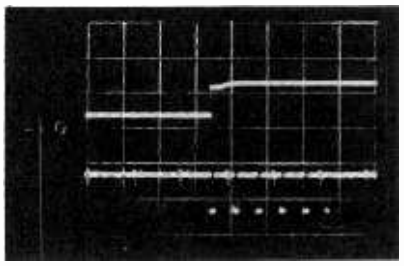
A. Top: Q7 base.
Bottom: P1-17 (TAPE SYNC), 2v/cm.



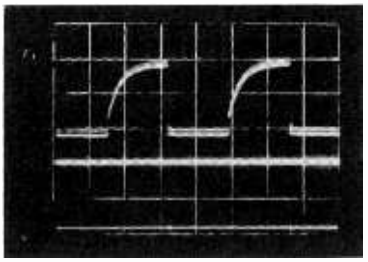
B. Top: Q7 emitter.
Bottom: Q7 base.



C. Top: Q6 collector, 1v/cm.
Bottom: Q7 emitter.



D. Top: Q10 collector.
Bottom: Q6 collector, 1v/cm.



E. Top: TP2 (VERT), 1v/cm.
Bottom: Tape Sync, 2v/cm.
(5 msec/cm)

Machine in STOP mode (MOD-DEMOD). All sweep times 50 μsec/cm, and amplitudes 5v/cm, unless otherwise noted.

Figure 47—Tape Vertical Sync Pulse Separator

waveform at the emitter of Q7 has been superimposed upon the waveform at its base so that the relationship between the cut-off bias voltage and the emitter signal may be seen. Note that the level of the cut-off bias voltage is sufficient to prevent any of the horizontal sync pulses from triggering Q7, while the greater amplitude pulse corresponding to vertical sync exceeds the bias voltage level and causes Q7 to conduct.

When transistor Q7 conducts, due to the integrated vertical sync signal at its base, it cuts off clamping transistor Q8. This removes the clamping action on the collector of differentiator transistor Q6, allowing the signal from Q8 to pass to the emitter of trigger amplifier transistor Q9. A signal appears at the collector of transistor Q6 only during the vertical sync interval, and the first pulse to appear is the boxcar

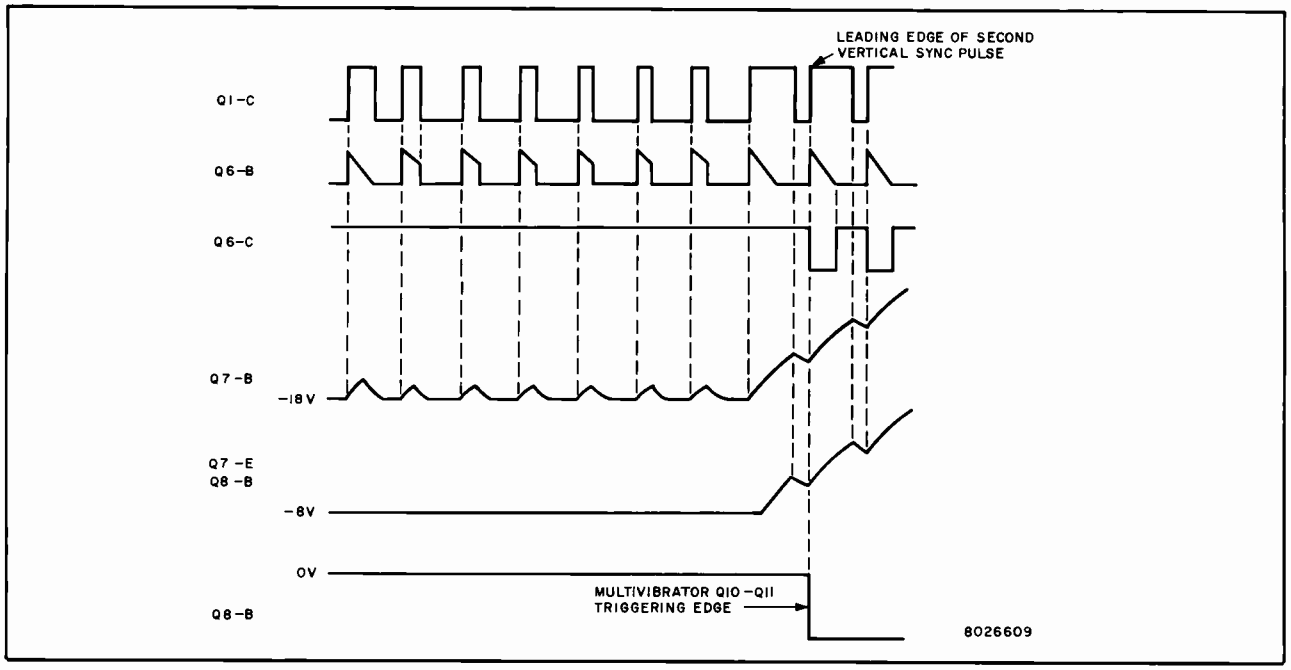


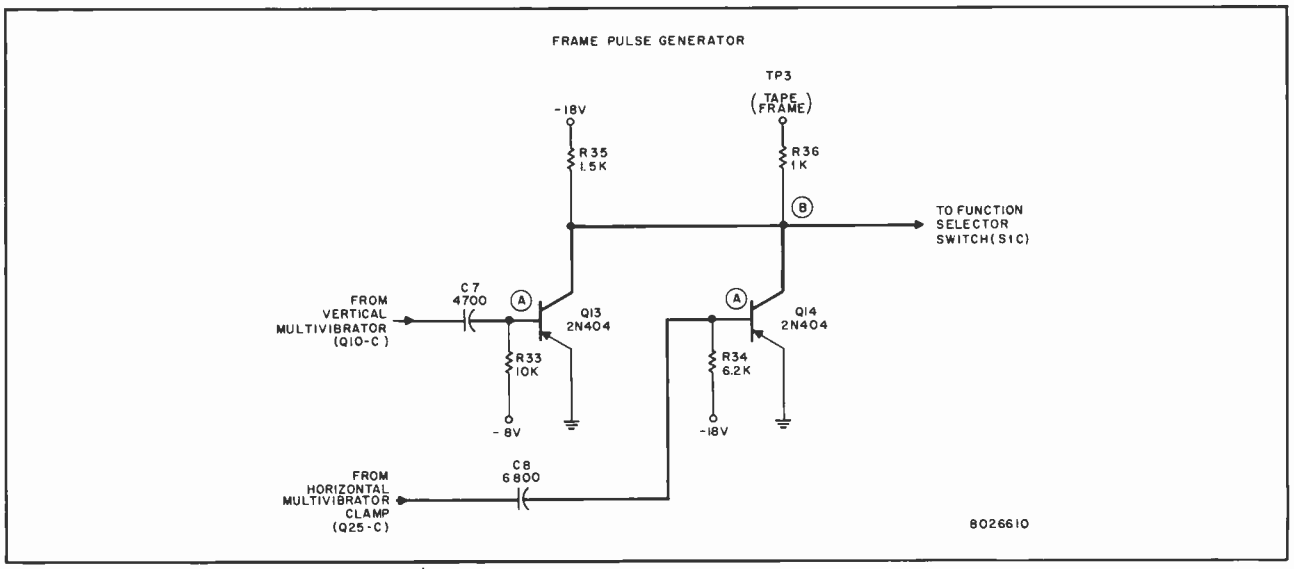
Figure 48—Waveforms Showing Development of Multivibrator Q10-Q11 Triggering Pulse

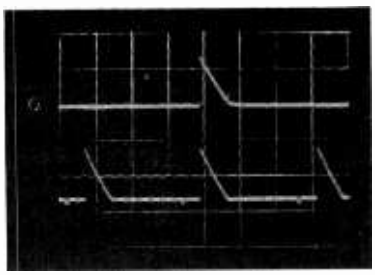
pulse derived from the leading edge of the second vertical sync pulse (figure 47C). Transistor Q9 operates as a common base amplifier, and its purpose is to amplify the signal from the collector of transistor Q6 without inverting it. When a negative-going pulse appears at the collector of transistor Q6, transistor Q9 is saturated and its collector clamps the potential at the junction of capacitor C6 and resistor R28 in the vertical multivibrator circuit at −9 volts. This places the full charge of capacitor C6 on the base of transistor Q10, which combines with transistor Q11 to form the vertical multivibrator, thereby cutting Q10 off and beginning the multivibrator action. Thus the vertical multivibrator is triggered in effect by the leading edge of the second vertical sync pulse, as shown in figures 47D and 48.

In the vertical multivibrator circuit the base of transistor Q10 is connected to ground through resistor R26, and the base potential is therefore positive with respect to the emitter potential; thus transistor Q10 is conducting in the multivibrator stable state. Simultaneously, transistor Q11 is cut off by the negative bias potential applied to its base from the voltage divider network consisting of resistor R30 returned to −18 volts and resistor R29 returned to the −8 volt potential at the collector of transistor Q10 when Q10 is conducting. The collectors of transistors Q9 and Q11 are at ground potential, and the base of transistor Q10 is at −8 volts, until a triggering pulse appears at the collector of transistor Q9. Thus capacitor C6 charges to the base potential of transistor Q10 during the interval between triggering pulses. When a triggering pulse occurs, the junction of capacitor C6 and resistor R28 is clamped at −9 volts and the full negative charge on C6 is applied to the base of transistor Q10, thus cutting the transistor off. Current is then supplied to the base of transistor Q11 through resistors R29 and R27 returned to ground, thereby driving Q11 into saturation. This action begins the one-shot period of the multivibrator, and the duration of the period is dependent upon the time constant determined by the values of resistor R26 and capacitor C6.

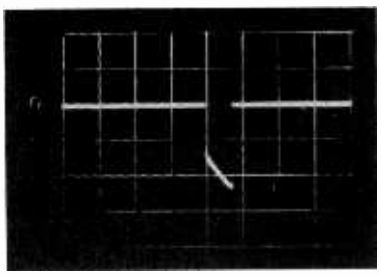
The signal at the collector of transistor Q11 is a negative pulse, having an amplitude of approximately 8 volts. This pulse is fed to vertical output transistor Q12, which operates as an emitter follower. Transistor Q12 provides the current gain necessary to drive the output signal, and also isolates the multivibrator from the output circuit. The tape vertical output signal at the emitter of transistor Q12 is fed from pin 29 of plug P1 to the linelock module (no. 316), where it is compared with the reference vertical sync signal to produce the tape vertical alignment (TVA) error voltage and to control the lock sense circuit. Test point TP2 (VERT) is provided for convenience in observing the tape vertical signal, which is shown in figure 47E.

The signal at the collector of transistor Q10 is a positive pulse, also having an amplitude of approximately 8 volts. This pulse is fed to the frame pulse generator circuit which is described below under the *Frame Pulse Generator* discussion.





A. Top: Q13 base.
Bottom: Q14 base.



B. Q14 collector.

Machine in STOP mode (MOD-DEMOD). All sweep times 20 μsec/cm and amplitudes 5v/cm.

Figure 49—Frame Pulse Generator

Frame Pulse Generator

Figure 49 shows the frame pulse generator circuit, which consists of transistors Q13-Q14 and associated circuit components. The positive-going tape vertical pulse from the collector of transistor Q10 in the vertical multivibrator circuit is differentiated by the network consisting of capacitor C7 and resistor R33. Transistor Q13, normally biased into saturation, is driven into cut-off by the positive-going edge of the differentiated tape vertical signal which is fed to its base (figure 49A). This action would normally produce a negative-going pulse at the collector of Q13; however, since transistor Q14 is also normally saturated (as described below) and transistors Q13 and Q14 have a common collector circuit, there will be an output signal only when both transistors are cut off simultaneously (coincidence).

The negative-going tape horizontal pulse from the collector of transistor Q4 in the horizontal multivibrator circuit occurs at a line frequency rate and is differentiated by the network consisting of capacitor C8 and resistor R34. The differentiated tape horizontal signal is fed to the base of transistor Q14 (figure 49A) which is normally biased into saturation. When the positive-going edge of the differentiated signal appears at its base, Q14 is driven into cut-off and would normally produce a negative-going pulse at its collector. As mentioned above, however, transistors Q13 and Q14 must be cut off simultaneously to produce an output pulse. Therefore, because of the half-line difference between fields, coincidence will only occur on every second field (once per frame). Thus the negative-going output pulse at the common collectors of transistors Q13 and Q14 will occur at a 30-cycle rate. This pulse is the tape frame pulse (figure 49B) and may be observed at test point TP3 (FRAME PULSE). The pulse is fed to the center-arm of switch S1C. When switch S1C is in switchlock (SL) or pixlock (PL) position, the pulse is fed through pin 28 of plug P1 to the capstan phase module (no. 320) where it is used in the reset pulse gating circuit. In the tone-wheel mode of servo operation, the tape frame pulse is not used.

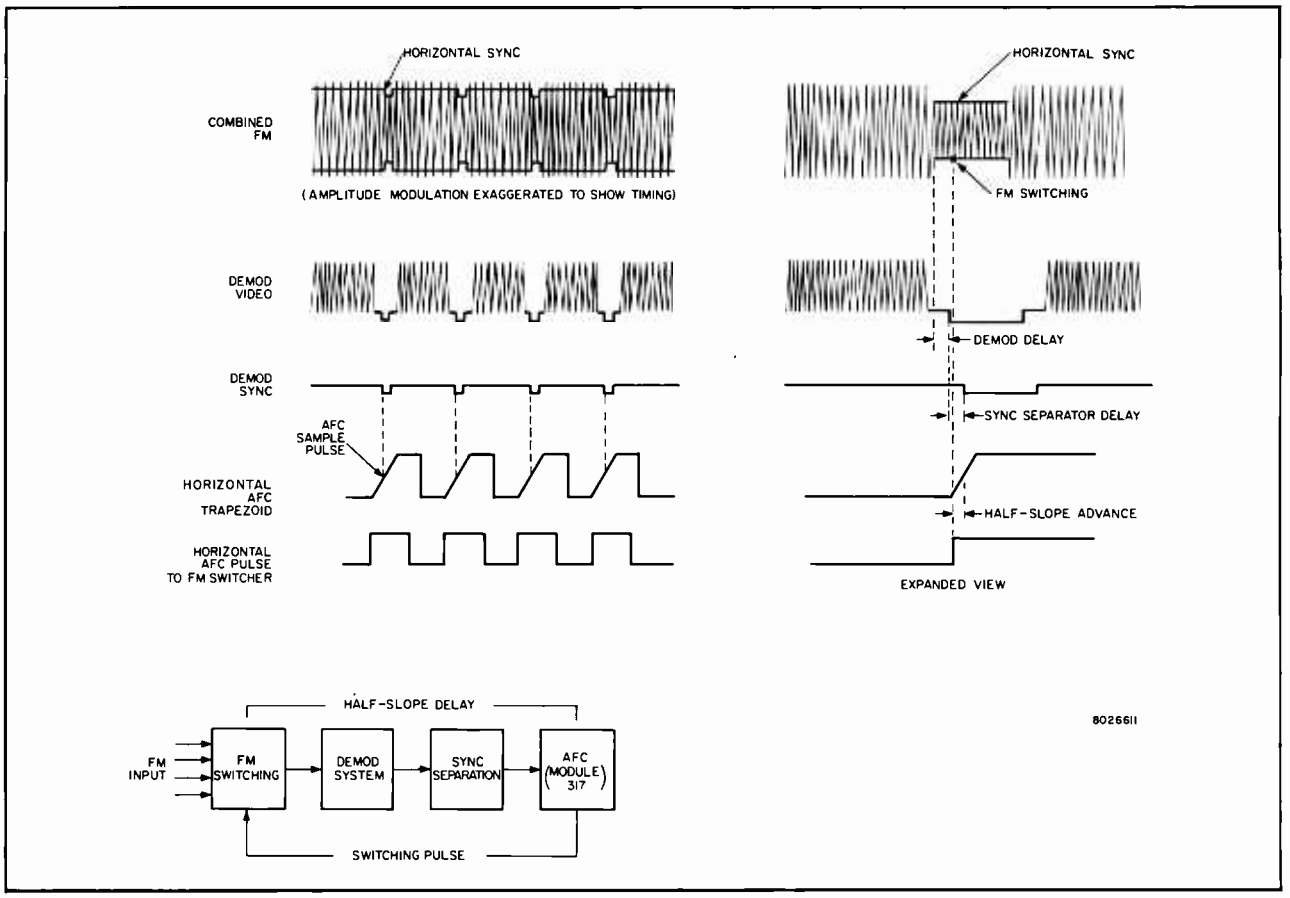


Figure 50—Development of Half-Slope Advance

Horizontal AFC Loop

The primary purpose of the horizontal afc loop is to provide the FM switcher circuitry with a waveform having an edge which is timed to tape horizontal sync but is advanced by a "half-slope" to insure that video head switching will always occur at a certain point within the horizontal sync interval (approximately one-third in from the leading edge). The half-slope advance compensates for the half-slope delay inherent in the circuitry from which the video head switching pulse is developed, and is obtained as shown in figure 50. In figure 50, the reference trapezoid waveform is generated from the afc multivibrator output, and occurs at a nominal rate of 15,750 cps. The pulse which samples the slope of the trapezoid waveform is developed from tape horizontal sync and therefore also occurs at a horizontal rate. As the frequency of the afc multivibrator changes slightly from that of tape horizontal sync, the sample pulse will appear to move up or down from a zero error mid-slope position. This movement causes an error signal to be developed which alters the frequency of the afc multivibrator, and thus that of the trapezoid waveform, to return the sample pulse to the center of the trapezoid slope. The video head switching pulse is also generated from the afc multivibrator output, and the leading edge of the switching pulse therefore coincides with the leading edge of the trapezoid waveform. In this manner the video head switching pulse is advanced by a half-slope with respect to the sample pulse which has been derived from tape horizontal sync.

Two supplementary functions are also performed by the afc loop. One of these functions is to provide an error signal to the guide servo module (no. 221). This signal contains a 960-cycle component which is utilized by the automatic guide servo circuitry to correct for "jogs" along the vertical edges of the picture. The second supplementary function is to provide a pulse, occurring at a line frequency rate, to the headwheel modulator module (no. 315) where it is utilized as the modulating pulse in controlling the headwheel motor speed.

The horizontal afc loop consists of a frequency controlled oscillator, trapezoid generator, sample pulse generator, diode comparator bridge (quad), and d-c error amplifiers.

A. Frequency Controlled Horizontal Oscillator

The horizontal oscillator (Q19-Q20-Q21) is an astable multivibrator which would normally "free run" at a frequency of 15.75 kc. However, in the horizontal afc loop the multivibrator frequency is actually controlled by an error signal developed from the comparison of its frequency with that of tape horizontal sync. Thus the multivibrator follows the tape horizontal sync frequency. In addition to the automatic frequency control feature, the multivibrator includes a manual frequency control and a self-starting circuit. The following paragraphs, in conjunction with figures 51 and 52, explain the operation of the oscillator circuit:

Assume transistor Q20 to be driven into saturation and transistor Q21 to be cut off. The collector of transistor Q21 is then at −18 volts, and the base of transistor Q20 is at ground potential. This condition allows capacitor C19 to charge to −18 volts with respect to the base of transistor Q20. Then, as transistor Q21 begins to conduct, its collector voltage immediately rises to ground potential and the voltage at the junction of resistors R68 and R69 is −9 volts. Since the voltage across capacitor C19 cannot change instantaneously, the base potential of transistor Q20 is forced to +9 volts (i.e., C19 is still charged to −18 volts with respect to the base of Q20). Transistor Q20 is then cut off and its collector voltage begins falling toward −18 volts. When the collector voltage of Q20 reaches −9 volts, capacitor C18 begins to charge toward −18 volts through resistor R57 and the collector voltage then continues to follow this slower time constant toward −18 volts. While the collector voltage of transistor Q20 is falling toward −18 volts, transistor Q21 is saturated and its base is essentially at ground potential.

Transistor Q20 will remain cut off as long as the voltage on its base remains positive. However, the positive voltage is due to the charge on capacitor C19, and this charge will leak off C19 through resistor R61 to the voltage at the emitter of emitter follower transistor Q19. Transistor Q19 conducts continuously due to the negative bias voltage applied to its base (as explained below); therefore, the voltage at its emitter is always at some negative value. Capacitor C19 will then attempt to charge to this negative value through resistor R61. At the instant the voltage on capacitor C19 goes slightly negative, transistor Q20 will be driven into conduction and C19 will be clamped at ground potential.

The charging of capacitor C19 from +9 volts toward the voltage at the emitter of transistor Q19 establishes the time interval of one half of the total multivibrator period. The second half of the period begins at the instant transistor Q20 conducts, and the sequence of operation is identical to that described above for the first half-period. The frequency of operation is inversely proportional to the sum of the two half-periods, and if potentiometer R62 (TAPE HOR FREQ SET) is adjusted correctly (with switch S2 on the front panel pressed), the frequency of the oscillator will be exactly 15,750 cps. (Refer to *Adjustments* for frequency adjustment procedure.)

Returning to the operation of emitter follower transistor Q19, it may be seen in figure 52 that one end of the voltage divider network comprised of resistors R60, R63 and potentiometer R62 is connected to the collector of either transistor Q20 or Q21 through diode CR5 or CR6 respectively, depending upon which diode is conducting. Forward bias is applied to the diode associated with whichever transistor is cut off and, since during normal operation only one transistor at a time is cut off, only one of the diodes will be conducting at any given instant. Therefore, one end of the voltage divider is always connected to the col-

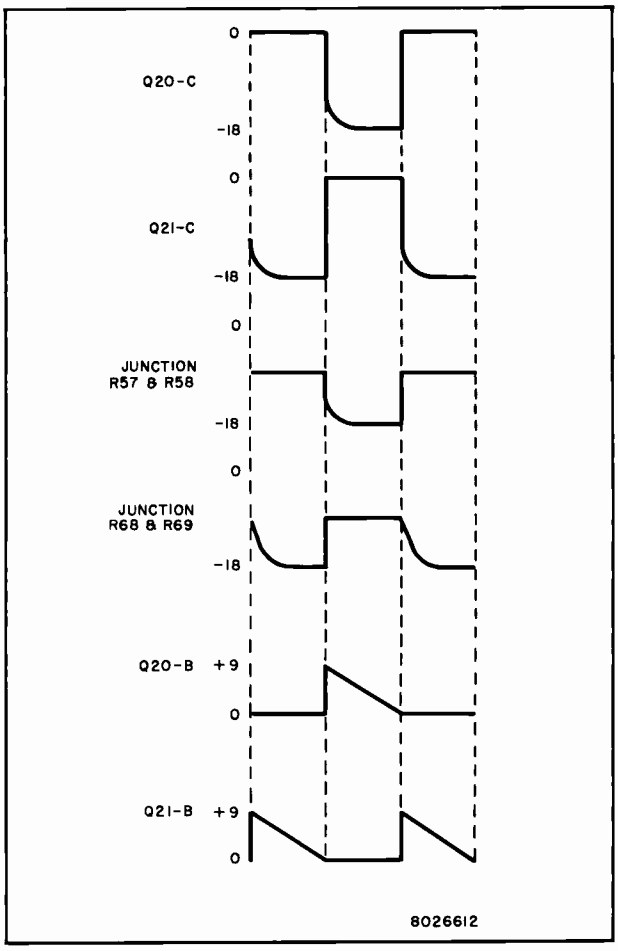
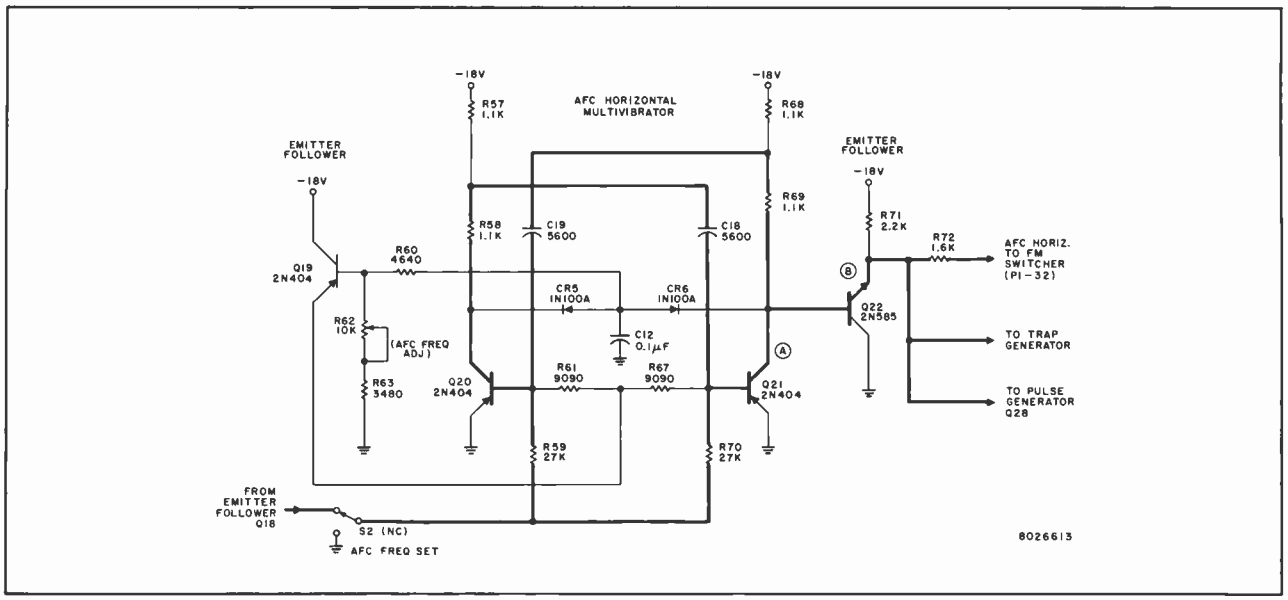
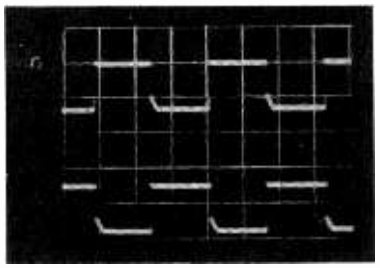
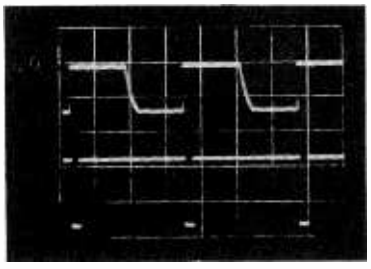


Figure 51—AFC Oscillator Circuit Waveform Relationships





A. Top: Q21 collector.
Bottom: Q20 collector.



B. Top: Q22 emitter.
Bottom: Tape Sync, 2v/cm.

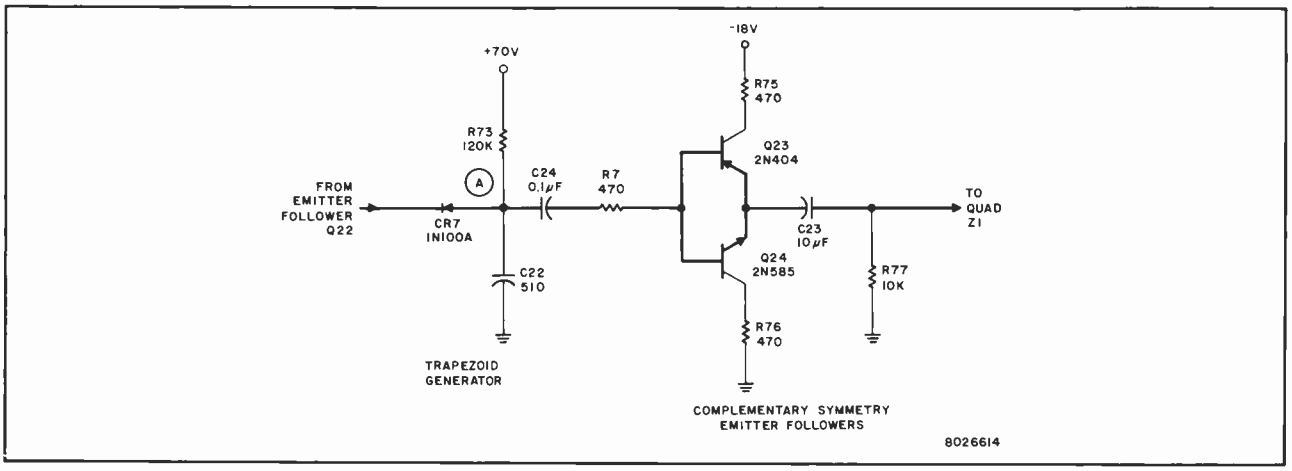
Machine in STOP mode (MOD-DEMOD). All sweep times 20 μsec/cm, and amplitudes 10v/cm, unless otherwise noted.

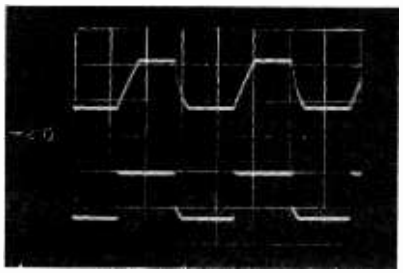
Figure 52—Frequency Controlled Horizontal Oscillator

lector of the transistor which is cut off, and the potential at that end of the divider consequently remains at approximately −18 volts. Potentiometer R62 is used to vary the negative voltage at the base of transistor Q19, thereby varying the negative emitter voltage which in turn determines the duration of one half of the multivibrator period. The purpose of emitter follower transistor Q19 then, is to isolate the loading effect of the base circuits of transistors Q20 and Q21 on the voltage divider, and to provide the base circuits with a low impedance source.

When the afc loop is closed, actual control of the oscillator frequency and phase with respect to that of the incoming tape horizontal sync signal is obtained by means of the current fed from emitter follower transistor Q18 to the base circuits of transistors Q20 and Q21 through resistors R59 and R70 respectively. This method of frequency control introduces a current into the oscillator charging circuits (C19, R61 and C18, R67) which is proportional to the horizontal frequency (15,750 cps). The injected current either adds to or subtracts from the normal charging currents, thereby altering the rate at which the capacitors (C18 and C19) charge toward the emitter potential of transistor Q19. As the rate of charge of each capacitor varies, the period of the multivibrator (and therefore the frequency of oscillation) changes. By utilizing this method of frequency control, any changes in the frequency of the tape horizontal sync will be followed by the oscillator.

The conventional astable multivibrator (i.e., a multivibrator having base resistors connected to the supply voltage) is not inherently self-starting because it is possible that both transistors may be saturated simultaneously and the circuit cannot then be regenerative. To achieve regeneration, and thus insure that multivibrator Q20-Q21 is inherently self-starting, the base resistors (R61 and R67) are connected to a supply voltage which is developed only when one or both transistors are cut off. Referring to figure 52, note that the supply voltage is developed by the circuit consisting of resistors R60 and R63, potentiometer





A. Top: CR7 anode, 5v/cm.
Bottom: Q21 collector, 10v/cm.

Machine in STOP mode (MOD-DEMOD). Sweep time: 20 μsec/cm.

Figure 53—Trapezoid Generator

R62, capacitor C12, transistor Q19, and diodes CR5 and CR6 connected to the collectors of transistors Q20 and Q21 respectively. From this circuit it may be seen that whenever transistors Q20 and Q21 attempt to saturate simultaneously, the voltage on base resistors R61 and R67 will be zero; therefore the base of each transistor is effectively grounded and the transistors cannot possibly saturate.

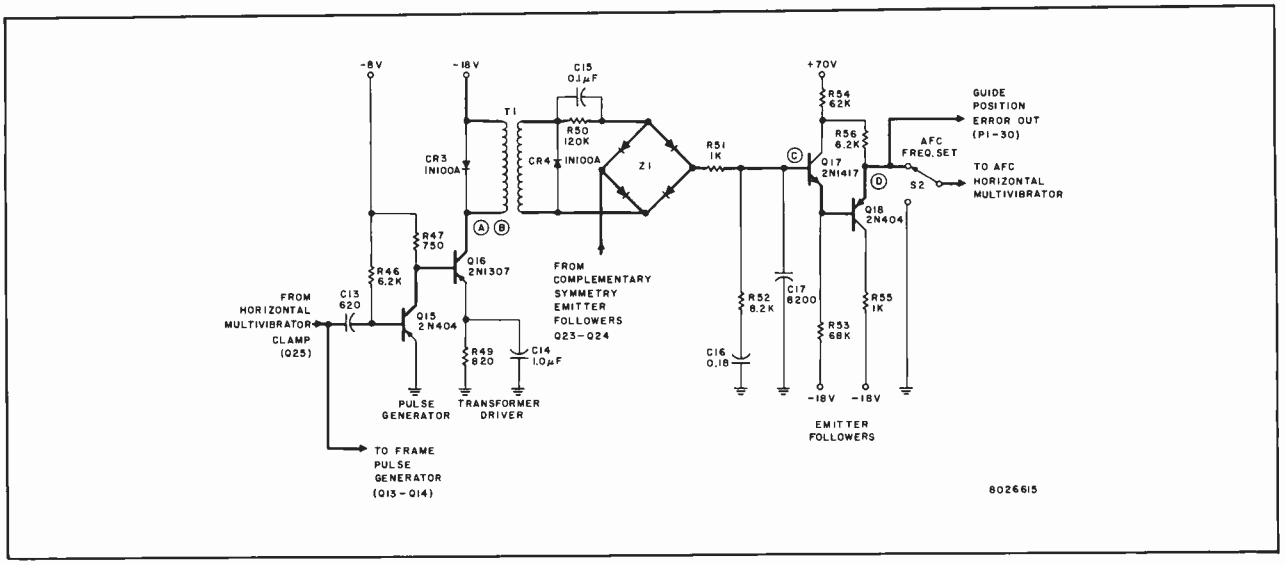
The signal at the collector of transistor Q21 (figure 52A) is fed directly to the base of emitter follower transistor Q22. Transistor Q22 lowers the impedance of the oscillator output and isolates the oscillator from the output circuits which follow. The pulse at the emitter of transistor Q22 (figure 52B) is fed to trapezoid and pulse generator circuits in this module and, via pin 32 of plug P1, to a 960H multivibrator circuit in the FM switcher module (no. 318).

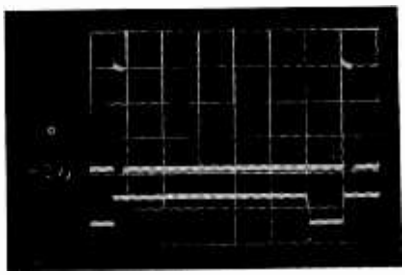
B. Trapezoid Generator

The trapezoid generator circuit consists of diode CR7, capacitor C22, and resistor R73 (figure 53). The purpose of this circuit is to produce a waveform having a linear slope of specified length from the positive-going edge of the 15.75 kc pulse output at the emitter of emitter follower transistor Q22.

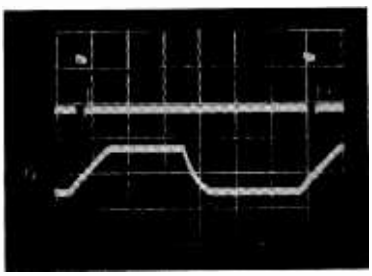
During the interval that transistor Q22 is cut off, its emitter potential is at approximately −14 volts dc. Diode CR7 is then forward biased and capacitor C22 is charged to −14 volts. When transistor Q22 is saturated, its emitter potential rises to ground. Since capacitor C22 is charged to −14 volts, diode CR7 is cut off. Capacitor C22 is then forced to discharge through resistor R73 toward +70 volts. As the potential at the junction of capacitor C22 and diode CR7 rises slightly above ground, the diode is again forward biased and the junction is clamped at ground potential for the duration of the saturation interval of transistor Q22. When transistor Q22 is driven into cut-off once again, its emitter potential falls to −14 volts and capacitor C22 charges rapidly to this potential through diode CR7.

The resulting trapezoid waveform (figure 53A), having a slope determined by the rate at which capacitor C22 discharges through resistor R73, is a-c coupled to the base circuit of the complementary symmetry emitter follower transistors Q23-Q24. These transistors reduce the impedance of the trapezoid generator circuit and provide sufficient current gain to drive comparator quad Z1.

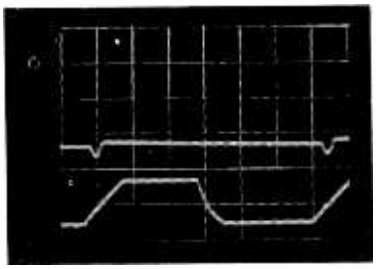




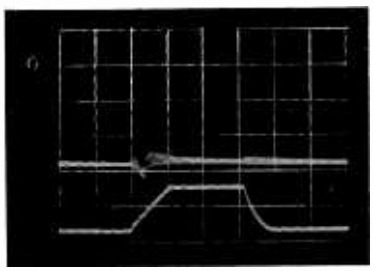
A. Top: Q16 collector, 5v/cm. Bottom: Q25 collector.



B. Top: Q16 collector. Bottom: Quad Z1 (green).



C. Top: Q17 base, 1v/cm. Bottom: Quad Z1 (green).



D. Top: Q18 emitter, 1v/cm. Bottom: Quad Z1 (green).

Machine in STOP mode (MOD-DEMOD). All sweep times 10 μsec/cm, and amplitudes 10v/cm, unless otherwise noted.

Figure 54—Sample Pulse Generator and Error Signal Amplifiers

C. Sample Pulse Generator and Error Signal Amplifiers

The trapezoid waveform, developed as described above, is sampled in a comparator bridge circuit by a sample pulse derived from the horizontal multivibrator output (figure 54). Capacitor C13 and resistor R46, in the pulse generating boxcar circuit of transistor Q15, form a network which differentiates the multivibrator output signal. The differentiated signal is fed to the base of normally saturated transistor Q15 and the positive-going edge of the signal drives Q15 into cut-off. When transistor Q15 is cut off, the potential at its collector falls toward −8 volts until it reaches a level which causes transformer driver transistor Q16, normally cut off, to be saturated. The collector potential of Q15 is then clamped at this level, for an interval determined by the values of resistor R46 and capacitor C13. The level at which the collector of transistor Q15 will be clamped depends upon the bias voltage developed at the emitter of transistor Q16.

This voltage in turn is determined by the repetition rate (15.75 kc) and duty cycle of the pulse output from transistor Q15, as well as by the current required by sample pulse transformer T1. The resulting output at the collector of transistor Q16 is a narrow, positive-going pulse which is timed to the positive-going edge of the output signal from the horizontal multivibrator (figure 54A). Diode CR3, in the collector circuit of transistor Q16, suppresses the inductive kick-back of the pulse transformer.

Pulse transformer T1 splits the phase of the sample pulse and drives opposite ends of comparator quad Z1 (figure 54). The quad is also driven by the trapezoid waveform, as mentioned above in the *Trapezoid Generator* discussion. During the interval between sample pulses, the quad is open (diodes cut off) and no signal flows to the quad output terminal. When a sample pulse appears, opposite ends of the quad are driven by pulses of opposite polarity and the quad is closed (diodes conducting). This allows the output voltage from the complementary symmetry emitter follower transistors Q23-Q24 to be fed through resistors R51 and R52 to storage capacitor C16.

If the afc horizontal oscillator is oscillating at the correct frequency (15.75 kc), the sample pulse will sample at the center of the trapezoid slope (figure 54B). Any variation in tape horizontal sync frequency will cause the sample pulse to shift in phase so that it will appear to move up or down on the trapezoid slope (depending upon whether the oscillator frequency is increasing or decreasing from 15.75 kc). As the sample pulse moves up on the trapezoid slope (i.e., in a positive direction), transistor Q23 in the complementary symmetry emitter follower circuit becomes biased at cut-off and transistor Q24 is biased into conduction. Capacitor C16 will then discharge toward ground potential through transistor Q24, when quad Z1 is conducting. Conversely, as the sample pulse moves down on the slope (i.e., toward −18 volts), transistor Q24 is biased at cut-off and transistor Q23 is biased into conduction. In this case, capacitor C16 charges toward −18 volts through transistor Q23 when the quad is closed. Therefore, during the sampling interval the voltage on capacitor C16 is a function of the tape horizontal sync frequency. After a sample pulse has occurred, the quad is again open (cut-off) and the charge on capacitor C16 remains essentially constant until the next sample pulse occurs. This action results in the generation of a d-c error signal which fluctuates at a horizontal rate. Since the afc loop has a 180-degree phase shift "built in", to avoid oscillation it is very important that there be no gain in the event that an additional 180-degree phase shift (regeneration) occurs. Capacitors C16, C17 and resistors R51, R52 form an "anti-hunt" network which establishes the loop gain characteristics, and the purpose of the network is to insure loop stability by shaping the loop gain characteristics for optimum afc action.

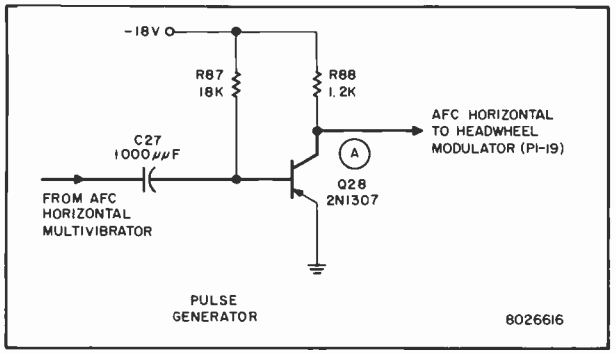
The d-c error signal thus generated is fed to emitter follower transistors Q17 and Q18 in cascade (figure 54C). The emitter follower transistors isolate the comparator quad from the afc horizontal oscillator, and provide the current gain necessary to drive the base circuits of the oscillator transistors Q20-Q21 through switch S2 (normally closed) and resistors R59 and R70 respectively.

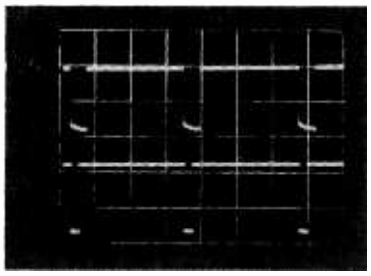
In addition to controlling the afc oscillator circuit, the error signal at the emitter of transistor Q18 (figure 54D) is fed through pin 30 of plug P1 to the guide servo module (no. 221) where it is utilized in positioning the vacuum guide during automatic guide servo operation. Since the horizontal afc circuit is a closed loop, whenever the tape horizontal sync rate varies from 15,750 cps an error signal is derived from the frequency difference (as mentioned above). If the guide servo does not correct for the change in frequency, the picture on the monitor will exhibit "jogs" along its vertical edges. The polarity of the slope of the jogs depends upon whether the tape horizontal sync frequency is too high or too low.

Switch S2 is a momentary contact pushbutton type which is inserted into the afc loop so that the loop may be opened when the afc horizontal oscillator frequency adjustment is made. The correct procedure for making the oscillator frequency adjustment is outlined under *Adjustments.*

AFC Horizontal Pulse Generator

Transistor Q28 and associated circuit components (figure 55) form a pulse generating boxcar circuit which develops a narrow, negative-going pulse at the horizontal rate (15.75 kc). The output waveform at the emitter of emitter follower transistor Q22 in the afc loop is differentiated by the network consisting of capacitor C27 and resistor R87. Transistor Q28, normally saturated, is driven into cut-off by the positive-going edge of the differentiated waveform fed to its base. When Q28 is cut off, its collector potential falls from ground to approximately −18 volts dc. Transistor Q28 will remain cut off for an interval which is determined by the time required for capacitor C27 to discharge through resistor R87 to the supply voltage (−18 volts dc).





A. Top: Q28 collector, 10v/cm.
Bottom: Tape Sync, 2v/cm.
(20 μsec/cm)

Machine in STOP mode (MOD-DEMOD).

Figure 55—AFC Horizontal Pulse Generator

The signal at the collector of transistor Q28 is thus a narrow, negative-going pulse (figure 55A) which occurs at a horizontal rate. The pulse is fed via pin 19 of plug P1 to the headwheel modulator module (no. 315) where it is used as a modulating pulse in controlling the headwheel motor speed.

Servo Mode Selector Switch

In addition to feeding the tape frame pulse to the capstan phase module during switchlock or pixlock servo modes, selector switch S1 performs several functions which are necessary to accomplish the transition from one servo mode to another (figure 56). (Figures 30 and 35 of the *TR-22 Television Tape Recorder Control and Power Supply Systems* instruction book, IB-31623, will prove helpful in determining the circuits controlled by sections A and B of S1.)

During machine operation in the PLAY mode, pin 18 of plug P1 is grounded through the SERVO REF pushbutton switch when the switch is in EXT mode. Under these conditions, if switch S1A is in TW or SL position no action takes place. However, if S1A is in PL position, ground potential is applied via pin 21 of plug P1 to the linelock module (no. 316). This activates the lock sense circuit, as explained in the linelock module circuit description. Therefore, under any conditions of machine operation other than tape playback using an external servo reference, the position of S1A has no effect on machine operation.

When the machine is operated in the PLAY mode the PLAY bus, and thus pin 6 of plug P1, is at ground potential. During tape playback with switch S1B in TW position then, no action takes place. With S1B in SL position, ground potential is applied via pin 4 of plug P1 to the tonewheel processor module (no. 313) and to the picture monitor switcher. In the tonewheel processor module, the ground potential is fed to the tonewheel indicator driver circuit which deenergizes the tonewheel indicator lamp (located above and to the left of the PLAY control panel and designated TW LOCK) when the machine is operated in the switchlock (or pixlock) servo mode, as explained in the tonewheel processor module circuit description. The ground potential is also fed from the tonewheel processor module to the switchlock (SW LOCK) indicator lamp causing the lamp to become illuminated, thus signifying machine operation in the switchlock servo mode. The ground potential fed to the picture monitor switcher appears at a spare switch position.

During tape playback in the pixlock servo mode, switch S1B is in PL position and ground potential is fed via pin 20 of plug P1 and the linelock module to the tonewheel processor and tonewheel servo modules. In the tonewheel processor module, the ground potential is applied to the tonewheel indicator driver circuit which deenergizes the tonewheel indicator lamp as mentioned in the above paragraph. The ground potential is also fed from the tonewheel processor module to the pixlock (PIXLOCK) indicator lamp, thus causing the PIX portion of the lamp to become illuminated at the instant S1 is rotated to PL position. (When the machine has attained a servo "lock", the LOCK portion of the pixlock indicator lamp will become illuminated as explained in the linelock module circuit description, thus signifying machine operation in the pixlock servo mode.) In the tonewheel servo module (no. 314), the ground potential enables a circuit which inserts a fixed delay into the tonewheel pulse path so that the tape vertical alignment (TVA) servo will correct for both positive and negative errors in the location of tape vertical sync with respect to reference vertical sync during tape playback in the pixlock servo mode, as explained in the tonewheel servo module circuit description. (The purpose in interlocking the ground connection through the linelock module when S1B is in PL position is to disable the TVA servo loop so that the machine cannot attempt to go into the pixlock servo mode if the linelock module is disconnected or removed from the machine.)

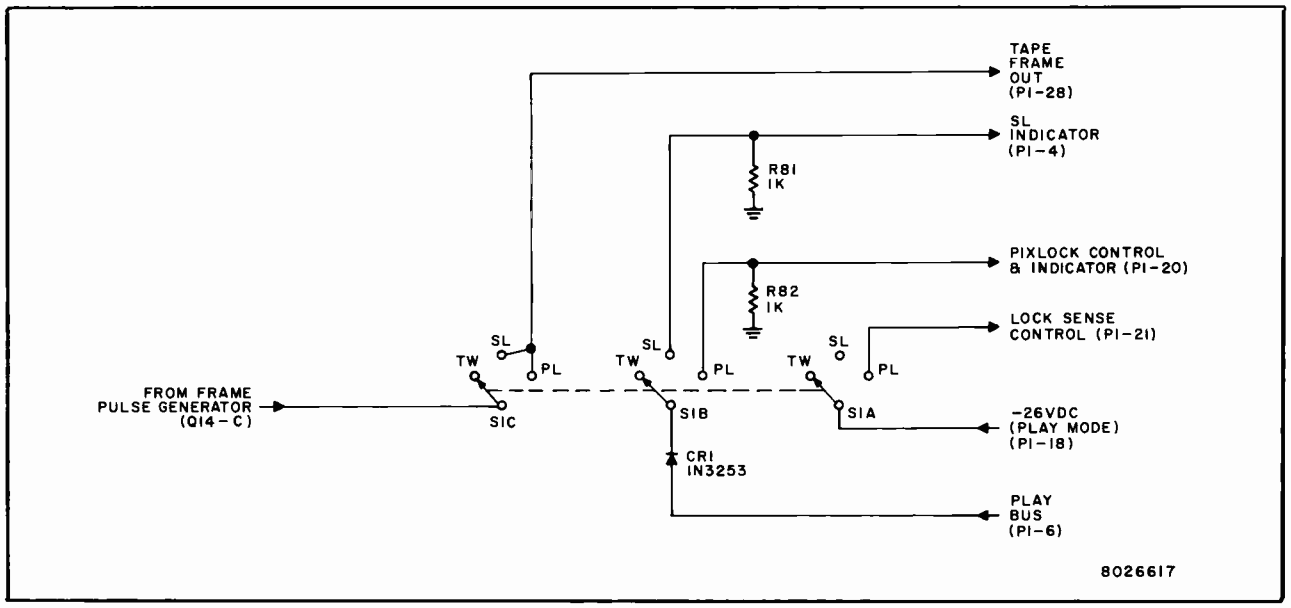


Figure 56—Servo Mode Selector Switch

Adjustments

The domestic version of the tape sync processor module has only one adjustment, and this is the "free-running" frequency of the horizontal oscillator in the afc loop. Two adjustment procedures are presented below. The first procedure outlines the proper method of obtaining the correct oscillator frequency while the second procedure is actually a "fine tuning", in that a method of obtaining the proper phase relationship is presented. Both procedures require a *Tektronix Type 535-A* oscilloscope or the equivalent.

A. Frequency Adjustment Procedure

1. Place machine in STOP mode, with DEMOD switch on PLAY control panel in MOD mode.

2. Place tape sync processor module on module extender.

3. Trigger oscilloscope internally on the positive-going edge of tape horizontal sync obtained from the HOR test point on the tape sync processor module.

4. Attach one of the oscilloscope probes to the HOR test point, and the other probe to the collector of transistor Q21 in the horizontal oscillator circuit. Adjust oscilloscope sweep to obtain a line-rate presentation (10 μsec/cm).

5. Press pushbutton on module front panel to open afc loop, and adjust TAPE HOR FREQ SET screwdriver control so that the positive-going edges of the waveform presentation on the oscilloscope are aligned.

6. To check frequency "lock", trigger oscilloscope externally (using the tape horizontal signal from the HOR test point) and observe alignment of waveform positive-going edges when the pushbutton is released. If the afc loop is "locked-in" correctly, alignment will be maintained when the pushbutton is released.

7. Replace module in machine.

B. Phase Adjustment Procedure

1. Play back a test tape with the SERVO REF switch in EXT mode and the function selector switch in TW position.

2. Trigger the oscilloscope "B" time base externally using tape vertical sync obtained from the VERT test point on the module front panel.

3. Attach an oscilloscope probe to one of the video output test points on the demodulator output module (no. 303), and adjust the oscilloscope "A" sweep to obtain a line-rate presentation (10 μsec/cm).

4. Using the oscilloscope sweep delay control, find one horizontal pulse in which switching appears during horizontal blanking.

NOTE: To make the appearance of switching more pronounced, operate the vacuum guide manually to reduce the tip penetration slightly, thus introducing a small amount of vacuum guide error.

5. Magnify the oscilloscope presentation and adjust the frequency screwdriver control slightly so that switching occurs one-third of the distance into horizontal sync (using the leading edge of the horizontal sync signal as a reference).

6. Correct any vacuum guide error introduced in step 4.

TAPE SYNC PROCESSOR MODULE (INTERNATIONAL)

Circuit Description

General

The International version of the tape sync processor module (no. 317) differs from the domestic version in that additional circuitry has been added to the International module to accommodate machine operation on any International line standard as well as on the domestic 525-line standard. Basically, the additional circuits accomplish the following functions: (1) cause the horizontal multivibrator duty cycle to remain essentially constant regardless of the line standard used; (2) cause the vertical separator integrator time constant to vary with line rate changes; and (3) cause the frequency of the multivibrator in the horizontal afc loop to vary in accordance with the line standard used.

The following paragraphs describe the operation of the circuits which accomplish the above functions; all other circuits contained in the International module operate as described in the domestic tape sync processor module discussion. Figure 57 is the block diagram of the International tape sync processor module.

Horizontal Multivibrator

The purpose of the monostable horizontal multivibrator circuit in the tape sync processor module is to remove all vertical components from the incoming tape sync signal during tape playback, and to thereby produce a pulse occurring at the horizontal rate from the tape sync signal. The horizontal multivibrator consists of transistors Q3 and Q4 (figure 58), and has a one-shot period whose duration is determined by the discharge rate of capacitor C3. The timed period exceeds that of half a TV line so that the multivibrator divides by two during the double rate pulses in the 9H interval of vertical blanking. Thus, the horizontal multivibrator removes all vertical components and produces a series of pulses occurring at the horizontal rate.

To compensate for the difference in horizontal frequencies between the various line standards, the discharge path of capacitor C3 varies according to the line standard selected (see figure 58). When the machine is to be operated on 405-, 525-, or 625-line standards, capacitor C3 is connected to the junction of resistor R9 returned to −8 volts and resistor R79 returned to the HN bus via pin 27 of plug P1. During 405-line operation, the HN bus is at ground potential. The equivalent resistance of the base circuit time constant of transistor Q3 is then essentially equal to the value of resistors R9 and R79 in parallel, and the Thevenin equivalent voltage is lower than −8 volts because of the fact that resistor R79 is returned to ground potential. This results in an increase in capacitor C3 discharge time, as compared with the discharge time of C3 when the machine is operated on 525- or

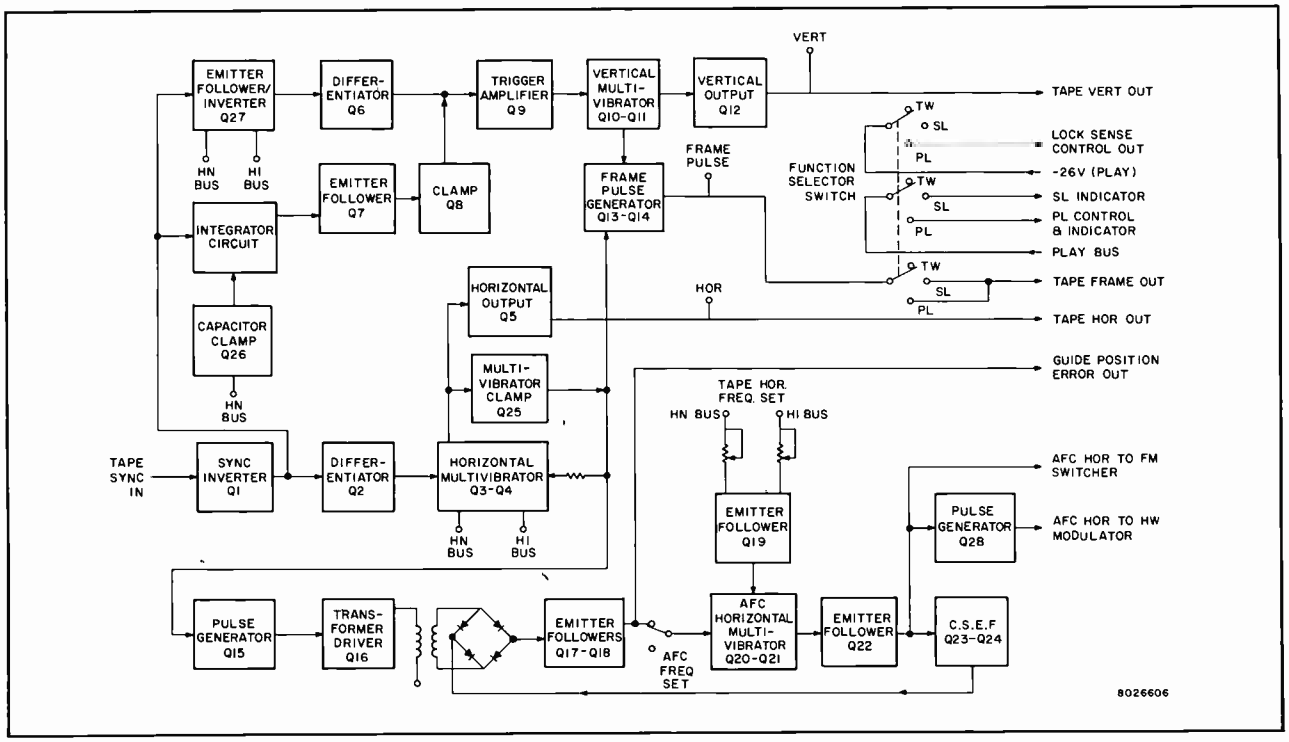


Figure 57—International Tape Sync Processor Module Block Diagram

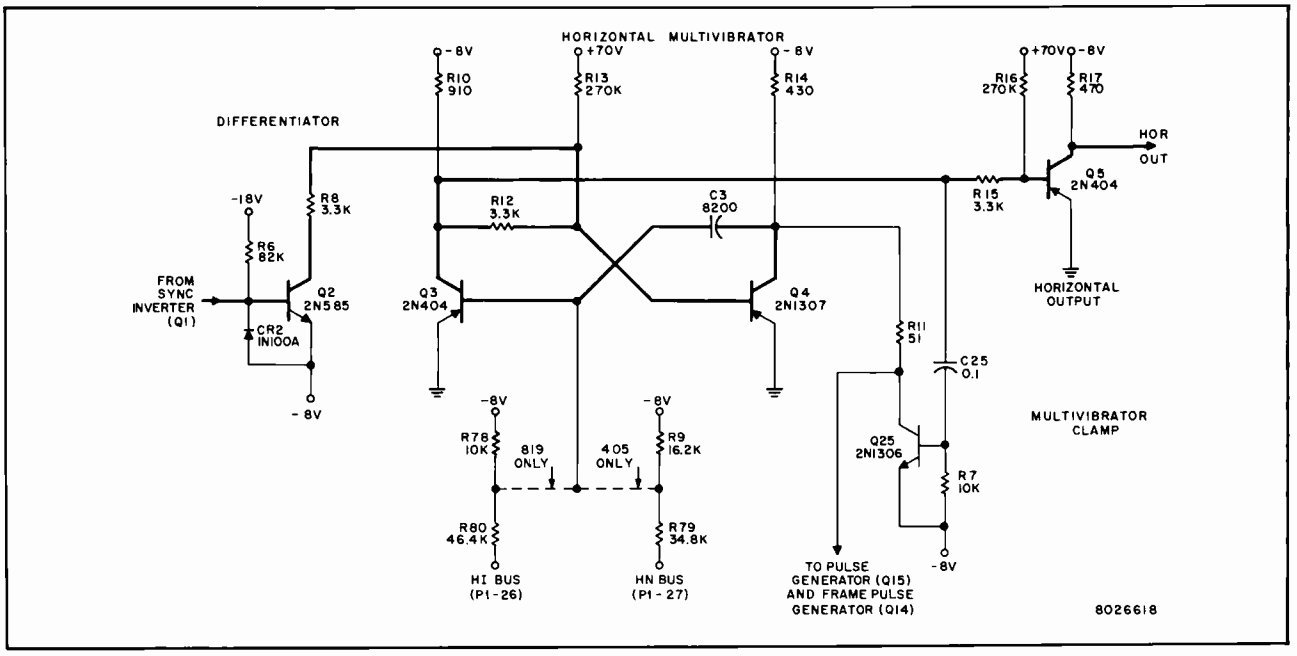


Figure 58—Horizontal Multivibrator

625-line standards and resistor R79 is returned to −20 volts via the HN bus.

When the machine is to be operated on 525-, 625-, or 819-line standards, capacitor C3 is connected to the junction of resistor R78 returned to −8 volts and resistor R80 returned to the HI bus via pin 26 of plug P1. During 525- or 625-line operation, the HI bus is at ground potential. The equivalent resistance of the base circuit time constant of transistor Q3 is then essentially equal to the value of resistors R78 and R80 in parallel, and the Thevenin equivalent voltage is lower than −8 volts because resistor R80 is returned to ground potential. In this case, the discharge time of capacitor C3 is increased during 525- or 625-line operation, as compared with 819-line operation when resistor R68 is returned to −20 volts via the HI bus.

The horizontal multivibrator time constant is thus switched in accordance with the various line standards, so that the multivibrator "on" time (unstable state) will be approximately the same percentage of a horizontal TV line regardless of the line standard used. Due to the relatively slight difference in horizontal frequency between the 525- and 625-line standards, it is unnecessary to alter the time constant when switching from one to the other of these standards.

Tape Vertical Sync Pulse Separator

The function of the vertical sync separator circuit in the tape sync processor module is to develop a pulse, timed with the leading edge of the second vertical pulse, during the vertical interval of the incoming tape sync signal. This pulse then triggers a multivibrator at the vertical rate, and the resulting output is the tape vertical sync signal. The tape vertical sync signal is utilized in the headwheel servo system in developing the tape vertical alignment (TVA) error signal and the lock sense control voltage, both of which are essential for tape playback in the pixlock servo mode. An additional use of the tape vertical sync signal is its function in deriving the tape frame pulse, which is utilized as a reset pulse in controlling binary counters in the capstan servo system when the machine is operating in the switchlock or pixlock servo mode.

The operation of the vertical sync separator circuit is described in detail in the domestic tape sync processor module discussion. Briefly, as shown in figure 59 differentiator transistor Q6, normally biased into saturation, is cut off by the positive-going portion of the signal fed to its base. When Q6 is cut off, its collector potential attempts to fall from −8 to −18 volts but is prevented from doing so by the clamping action of transistor Q8. Transistor Q8 is normally biased into saturation and its collector potential, and thus the potential at the collector of transistor Q6, will remain at −8 volts until a positive-going pulse from emitter follower transistor Q7 cuts Q8 off. The positive-going pulse appears at the base of transistor Q8 when transistor Q7, normally cut off by the biasing arrangement in its base circuit, is driven into conduction by the positive-going portion of the integrated tape sync signal fed to its base.

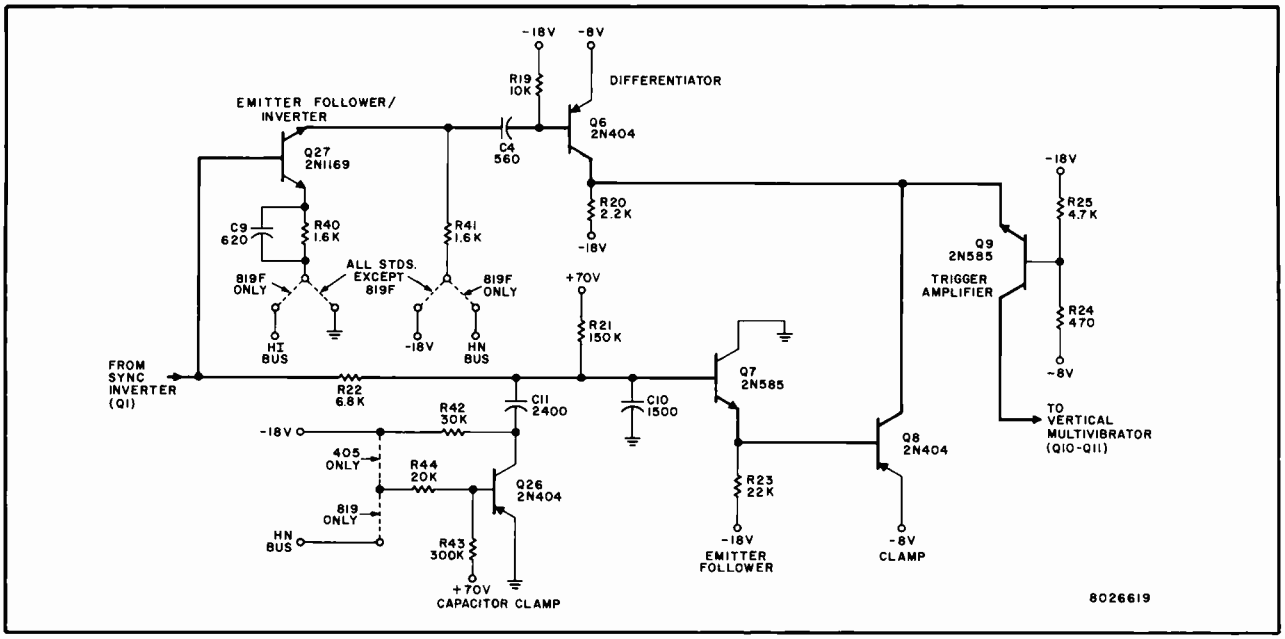


Figure 59—Tape Vertical Sync Pulse Separator

To obtain vertical sync separation, the time constant of the integrator network in the base circuit of transistor Q7 must be such that the integrator network output charges to approximately 80% of its maximum amplitude within a period equal to that of one half of a TV line. Thus the amplitude of the integrator network output is too low to drive transistor Q7 into conduction when horizontal sync appears, but is sufficiently high to drive Q7 into conduction when vertical sync appears. Since the time constant of the integrator network is a function of the line rate, or horizontal frequency, the International tape sync processor module contains circuitry which compensates for the relatively large difference in horizontal frequency between machine operation on 405-, 525-, or 625-line standards and machine operation on 819-line standards.

As shown in figure 59, transistor Q26 operates as a switch which controls the function of capacitor C11 in the integrator circuit. When the machine is to be operated on 405-, 525-, or 625-line standards, resistor R44 in the base circuit of transistor Q26 is returned to −18 volts. The voltage divider network consisting of resistor R44 and resistor R43 returned to +70 volts biases transistor Q26 into saturation. The collector of Q26 is then at ground potential and capacitor C11 is in parallel with capacitor C10. If the machine is to be operated on 525-, 625-, or 819-line standards, resistor R44 is returned to the potential on the HN bus. When the machine is operating on 525- or 625-line standards, the HN bus potential is −20 volts. Therefore transistor Q26 is again saturated, and capacitor C11 is in parallel with capacitor C10. However, when the machine is operating on 819-line standards, the HN bus is at ground potential. Transistor Q26 is then biased at cut-off, and capacitor C10 is effectively disconnected from the integrator circuit. Thus the integration of sync is decreased to accommodate the comparatively narrow sync pulse and faster line rate occurring when the machine is operated on 819-line standards.

In addition to the modifications noted above, the International tape sync processor module contains a circuit which permits machine operation on 819-line French standards (819F) as well as on the normal International and domestic standards. The additional circuitry consists of emitter follower/inverter transistor Q27 and associated circuit components (figure 59), and its purpose is to pass the signal from sync inverter transistor Q1 without inverting it during machine operation on all line standards except 819F and to invert the signal when the machine is operating on 819F standards. This inversion during 819F standards is necessary for the separation of the single, very short, unserrated vertical sync pulse which occurs in the 819-line French system (see figure 60).

Transistor Q27 is a bilateral type (i.e., either electrode may function as emitter or collector). During machine operation on all line standards except 819F, resistor R41 is returned to −18 volts and resistor R40 is returned to ground potential. The upper electrode of transistor Q27 (figure 59) then acts as the emitter and the lower electrode as the collector; thus the

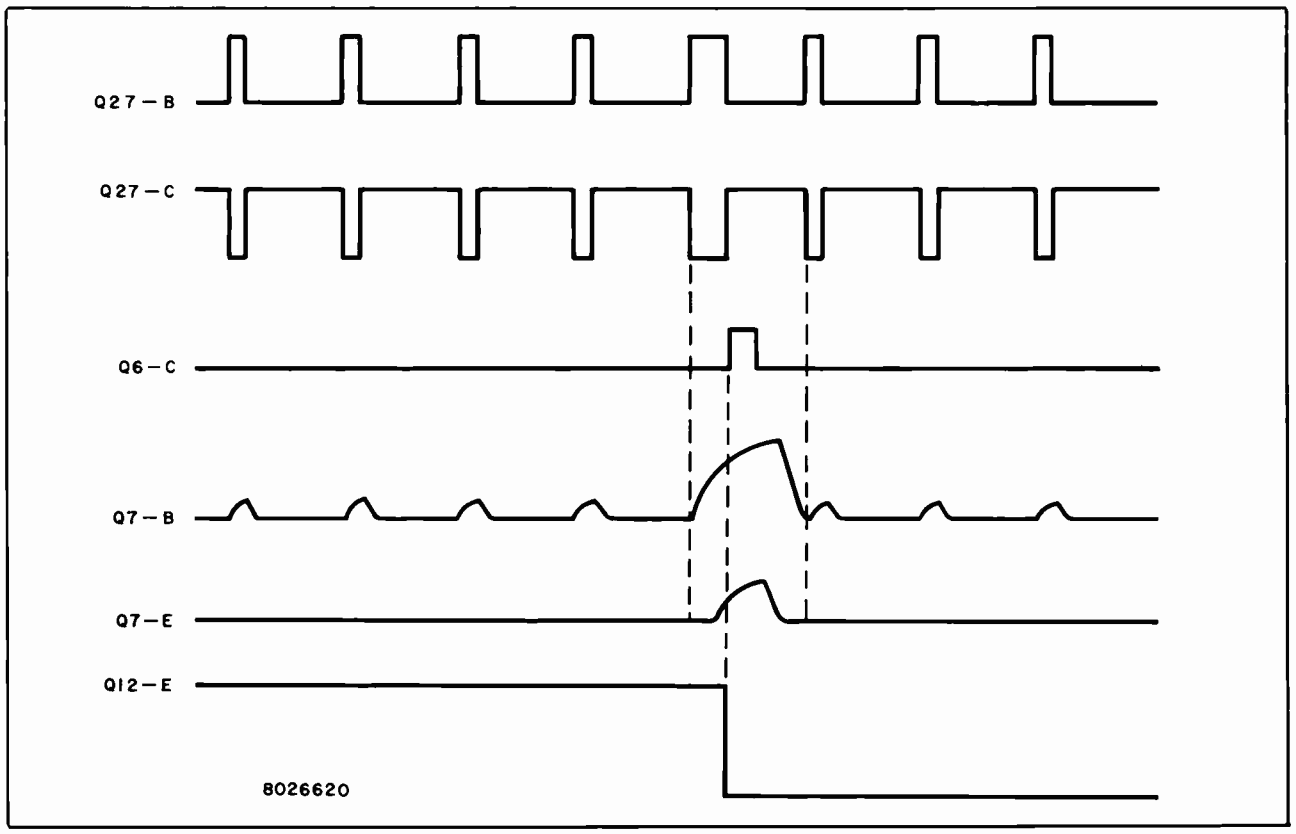


Figure 60—Vertical Sync Separation in 819-Line French System

transistor operates as an emitter follower and the signal at its emitter appears exactly as does the signal at its base. During machine operation on 819F standards, resistor R41 is returned to ground via the HN bus and resistor R40 is returned to −20 volts via the HI bus. This causes the upper electrode of transistor Q27 to act as the collector and the lower electrode as the emitter; thus the signal appearing at the collector (upper electrode) of transistor Q27 is inverted with respect to the signal at its base.

Horizontal AFC Loop

The primary purpose of the horizontal afc loop is to provide the FM switcher circuitry with a waveform having an edge which is timed to tape horizontal sync but is advanced by a specified amount to insure that video head switching will always occur at a certain point within the horizontal sync interval (approximately one-third in from the leading edge). Supplementary functions performed by the afc loop include the generation of an error signal containing a 4XTW cps component, which is utilized by the guide servo circuitry, and the generation of a pulse occurring at a line frequency rate, which is utilized as the modulating pulse in controlling the headwheel motor speed.

The heart of the afc loop is the frequency controlled horizontal oscillator, which is an astable multivibrator oscillating at a nominal frequency of 15,750 cps in the domestic tape sync processor module. A detailed explanation of the horizontal oscillator operation is provided in the domestic module circuit description, and should be referred to in order that the following discussion may be more clearly understood.

In the International tape sync processor module, the horizontal oscillator frequency is changed to correspond to the line standard selected by switching the voltage divider resistance in the base circuit of emitter follower transistor Q19 (figures 61 and 62). Since transistor Q19 operates as an emitter follower, a voltage variation at its base will also appear at its emitter and thus result in a current variation in the base circuits of transistors Q20 and Q21. Therefore, a change in potential at the base of emitter follower transistor Q19 will alter the period of multivibrator Q20-Q21 and thus the frequency at which it oscillates. (See figure 63.) The following paragraphs, in conjunction with figures 61 and 62, explain the manner in which the voltage divider network is switched to accommodate the different line standards. Note in figures 61 and 62 that the circuit connections differ between International modules to be used in machines

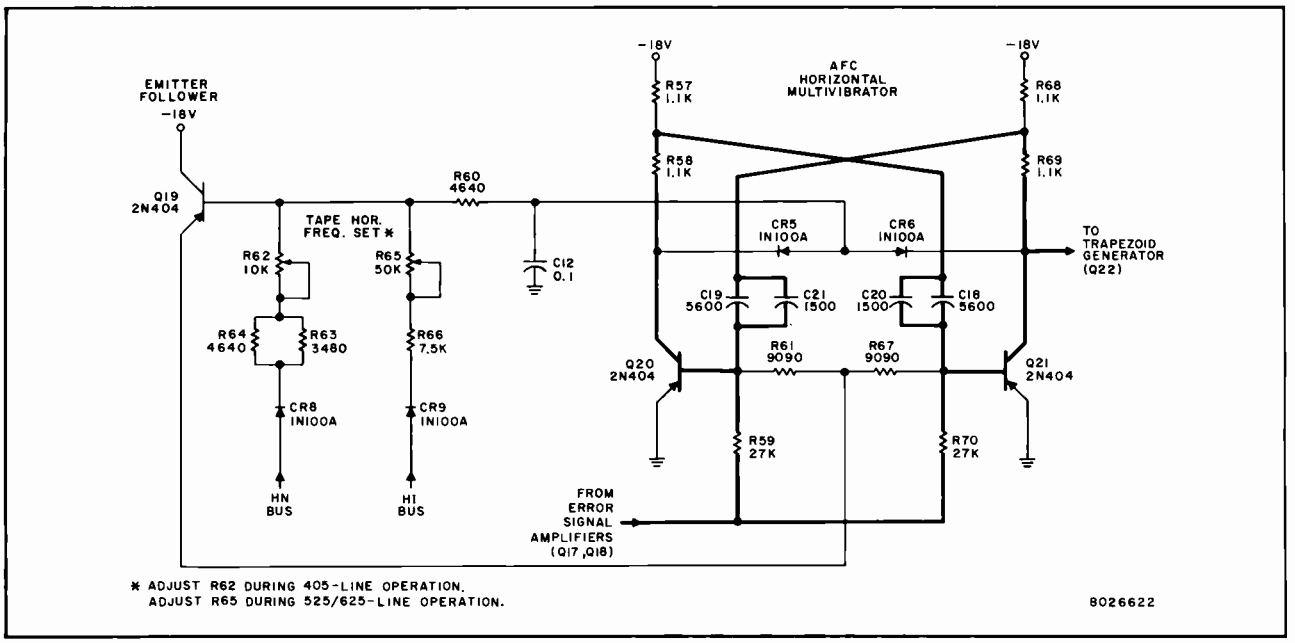


Figure 61—Horizontal Oscillator (405-, 525-, 625-Line Standards)

operating on 405-, 525-, and 625-line standards and those to be used in machines operating on 525-, 625-, and 819-line standards.

In the 405-, 525-, 625-line sequence, diode CR8 is connected to the HN bus and diode CR9 is connected to the HI bus (see figure 61). When the machine is operated on 405-line standards the HI bus is at −20 volts; thus diode CR9 is reverse biased and resistor R66 and potentiometer R65 are effectively disconnected from the oscillator timing circuit. Simultaneously, the HN bus is at ground potential; thus diode CR8 is forward biased and resistors R63-R64 in parallel and potentiometer R62 are connected into the timing circuit. Therefore, during machine operation on 405-line standards the active voltage divider elements in the base circuit of transistor Q19 are resistors R63-R64 in parallel, potentiometer R62, and resistor R60 connected to the collector of whichever transistor (Q20 or Q21) is cut off (by either diode CR5 or CR6). This network establishes the period of multivibrator Q20-Q21, and thus the frequency of oscillation. Potentiometer R62 is then utilized in fine tuning the oscillator to obtain the exact center frequency (with zero error signal). When the machine is operated on 525- or 625-line standards, the potentials on the HN and HI busses are reversed. Diode CR8 is then reverse biased and diode CR9 is forward biased, so that the active voltage divider elements in the base circuit of transistor Q19 are now resistor R66, potentiometer R65, and resistor R60 returned to the collector of whichever transistor is cut off (Q20 or Q21). In this case potentiometer R65 is utilized in obtaining a fine frequency adjustment. It should be noted that in the 405-, 525-, 625-line sequence, capacitor C21 is connected in parallel with capacitor C19 and capacitor C20 is connected in parallel with capacitor C18, thus increasing the capacitance in the timing circuit during machine operation on 405-, 525-, and 625-line standards with respect to the timing circuit capacitance during 525-, 625-, and 819-line machine operation.

In the 525-, 625-, 819-line sequence, diode CR8 is connected to the HI bus and diode CR9 is connected to the HN bus (see figure 62). When the machine is operated on 525- or 625-line standards, the HI bus is at ground potential and the HN bus is at −20 volts. Thus diode CR9 is reverse biased and diode CR8 is forward biased, so that the active voltage divider elements in the base circuit of transistor Q19 are resistor R63, potentiometer R62, and resistor R60 returned to the collector of whichever transistor is cut off (Q20 or Q21). Potentiometer R62 is utilized in making the fine frequency adjustment when the machine is operating on 525- or 625-line standards. If the machine is operating on 819-line standards, the potentials on the HI and HN busses are reversed, thus cutting off diode CR8 and forward biasing diode CR9. The active voltage divider elements in the base circuit of transistor Q19 will then be resistor R66, potentiometer R65, and resistor R60 returned to the collector of whichever transistor is cut off (Q20 or Q21). Thus when operating the machine on 819-line standards, the fine frequency adjustment is made by utilizing potentiometer R65.

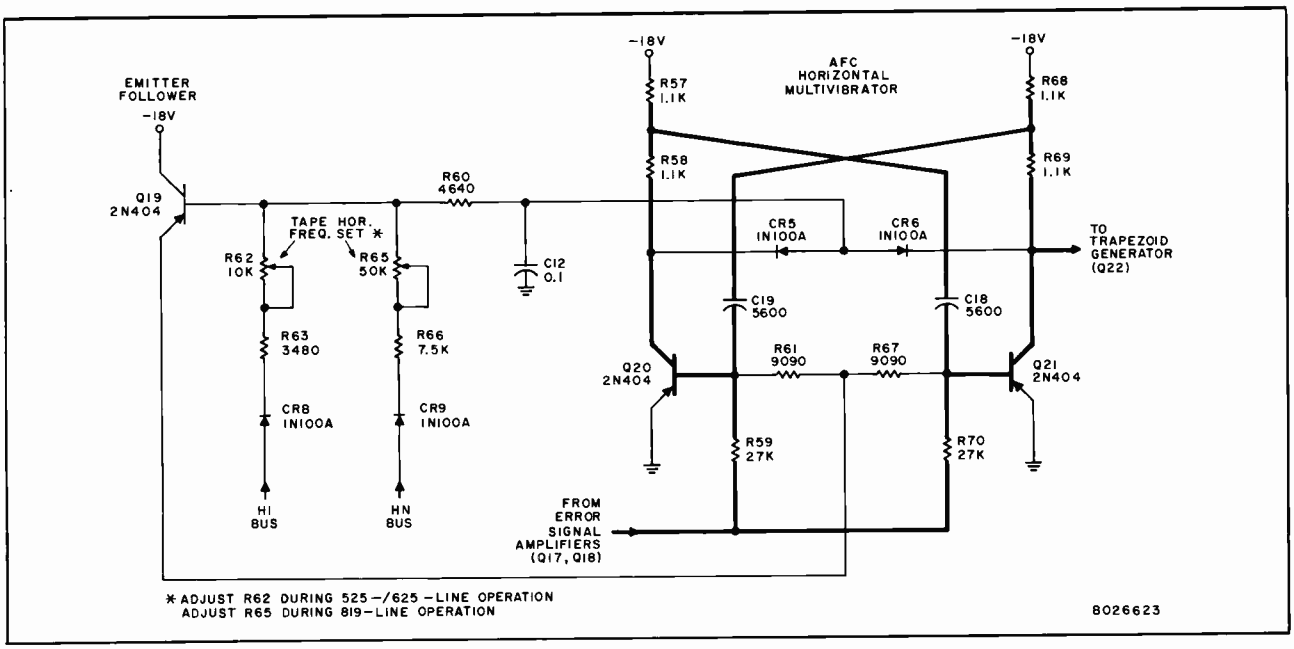


Figure 62—Horizontal Oscillator (525-, 625-, 819-Line Standards)

From the above discussion of the horizontal oscillator timing circuit it may be seen that when connections are made in the International tape sync processor module for the 405-, 525-, 625-line sequence, potentiometer R62 is utilized in making the fine frequency adjustment during 405-line operation, and potentiometer R65 is utilized during 525- or 625-line operation. Also, when connections are made for the 525-, 625-, 819-line sequence, potentiometer R62 is utilized in making the fine frequency adjustments during 525- or 625-line operation, and potentiometer R65 is utilized during 819-line operation. Thus potentiometer R65 is utilized in making the fine frequency adjustment when the machine is operating on the higher frequency line standards, regardless of the line standard sequence. The coarse frequency "adjustment", or line standard switching, is accomplished by utilizing the potentials on the HN and HI busses. To adjust the horizontal oscillator frequency properly in the International module, follow the procedure outlined in the *Adjustments* section of the domestic tape sync processor module description.

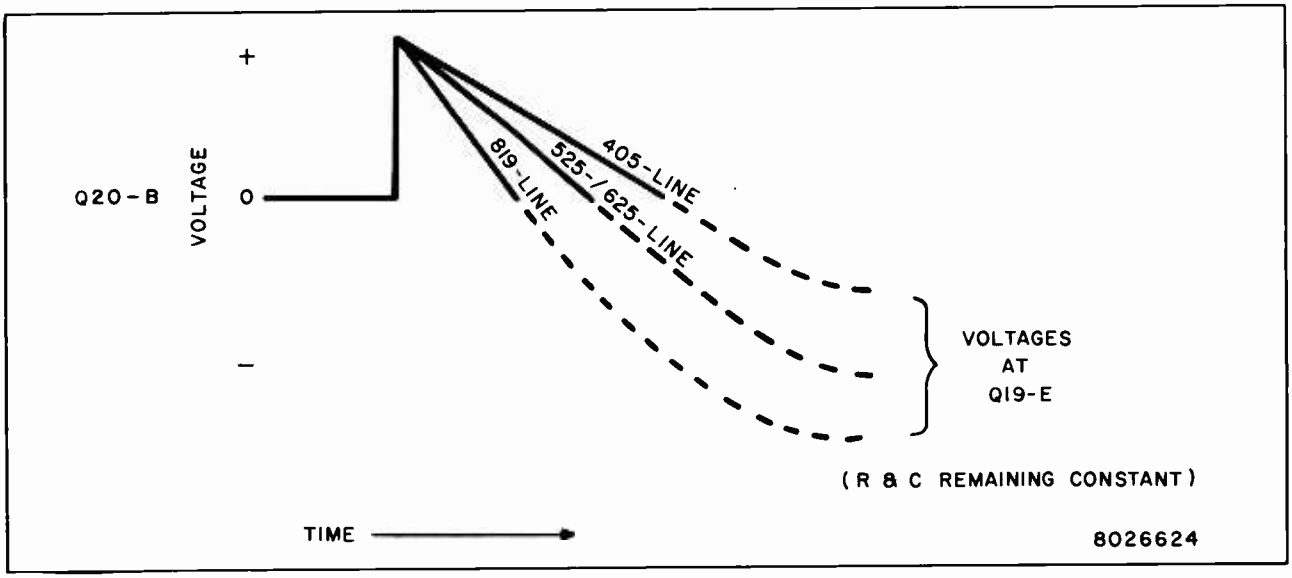


Figure 63—Waveforms at Base of Transistor Q20 Showing Relationship Between Voltage at Emitter of Transistor Q19 and Half-Cycle Period of Horizontal Multivibrator

CAPSTAN SERVO

SYSTEMS DESCRIPTION

GENERAL

The purpose of the capstan servo system is to control the speed of the capstan motor and thus the speed at which the tape runs through the machine. The linear tape speed is nominally 15 inches-per-second (15.625 ips in International machines), however during tape playback it is necessary that the capstan motor speed be tightly controlled to insure that exactly four video tracks are pulled past the rotating headwheel assembly during each rotation of the headwheel.

The capstan servo system consists of the following modules in addition to the capstan motor itself:

Control Track REC/PB (no. 319)
Capstan Phase (no. 320)
Capstan Error (no. 321)
Capstan Oscillator (no. 322)
Capstan Power Amplifiers (nos. 330 and 331)

NOTE: If the machine is to be operated on International standards, the capstan phase module must be replaced with a special International version. This version is similar in outward appearance to the domestic module, however it contains circuitry which compensates for certain timing differences between the standards.

The following discussion of the capstan servo system presents a brief overall description of the system operation during tape recording and playback. (For a more detailed explanation of a particular area, refer to the individual module circuit descriptions.) In the systems discussion, all timing references pertain to machine operation on domestic (525-line) standards. If the machine is operated on International standards, the appropriate timing differences must be taken into consideration (e.g., substitute 50-cycle for 60-cycle; 250-cycle for 240-cycle; etc.). The *Capstan Servo System Functional Diagram* (figure 126 at the rear of this instruction book) will prove helpful in visualizing the overall system operation.

NOTE: Throughout the following discussion of the Capstan Servo System, reference is frequently made to a "frame" pulse. In the tape recording and playback processes there are actually two separate and distinct series of pulses, each series occurring at a frame rate; i.e., 30 cps (25 cps in International machines). One series is obtained by comparing *station* (reference) horizontal and vertical sync signals in a coincidence gate circuit. The resulting pulses are then superimposed upon the control track signal and the combined signal is recorded along the bottom edge of the tape. The characteristics of this signal are specified by the SMPTE recommended practices, and the pulse (sometimes referred to as the "edit" pulse) is used as a frame marker during tape editing to produce "roll-free" splices. This pulse has no functional purpose in machine operation after it has been recorded on the tape, and will be designated the "control track-frame pulse" in the following text.

The second series of pulses is derived from tape video information obtained from the video heads. In this case, *tape* horizontal and vertical sync signals are compared in a coincidence gate circuit and the resulting pulse thus bears a definite relationship to the tape video signal. This pulse is used by the machine during switchlock or pixlock servo operation and its function is described in detail in this instruction book. The pulse is referred to in the following text as the "video-tape frame pulse".

RECORD Mode

In order to maintain a definite timing relationship between tape movement and video head scanning during the recording process, the capstan motor speed is "locked" to that of the headwheel motor. This is accomplished by utilizing the tonewheel pulse in triggering a chain of binary counters which divide down the 240-cycle tonewheel pulse frequency to produce the 60-cycle signals that drive the 2-phase, synchronous capstan motor. Because the tonewheel is physically attached to the headwheel motor shaft, both the tonewheel and the headwheel rotate at the same speed. Therefore, since the frequency of the signals driving the capstan motor will follow that of the tonewheel pulse, a "lock" is established between the capstan and headwheel motors. This method of controlling the capstan motor speed insures that the tracks laid down on the tape during recording follow a standard geometrical pattern (e.g., that specified by the SMPTE or CCIR), thus facilitating interchangeability of tapes.

NOTE: In the RECORD mode, the headwheel motor must lock-in at its correct speed before the tonewheel pulse is applied to the first binary counter. Until a headwheel lock has been attained, the counter is driven by the 240-cycle local oscillator used during tape playback. This arrangement protects against excessive motor and power amplifier circuit currents during start-up.

The binary counters produce two 60-cycle signals differing in phase by 90 degrees. (See block diagram, figure 64, and functional diagram, figure 126.) The phase relationship between the 60-cycle signals is determined by a diode gating circuit and is such that the capstan motor will always run in a clockwise direction. The 60-cycle, phase-split output signals from the

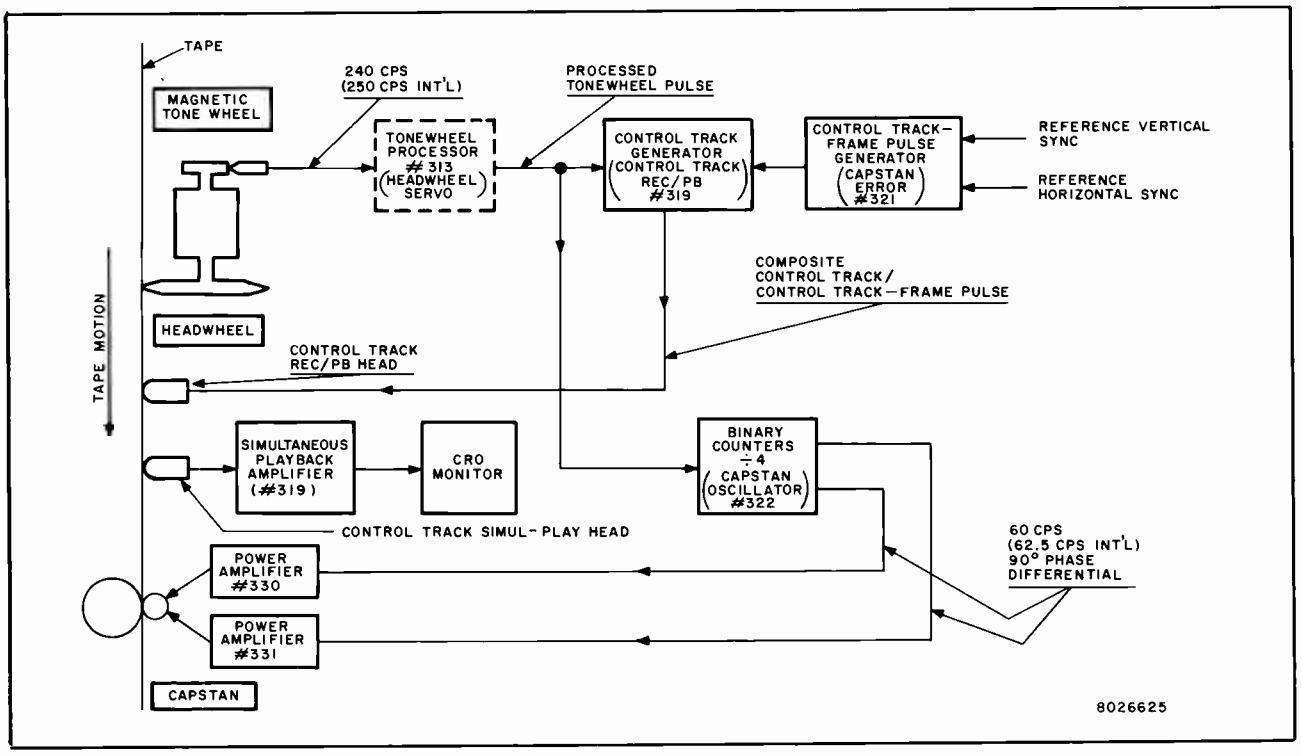


Figure 64—Capstan Servo System (RECORD Mode)

binary counters are converted into sinusoidal signals and fed to separate power amplifiers which provide the power required to drive the capstan motor.

To provide a continuous accurate record of the capstan motor speed during recording, a 240-cycle sinusoidal control track signal is recorded along the lower edge of the tape by the control track head located on the headwheel panel. (The control track is utilized in controlling tape motion during playback, and is analogous to the sprocket holes in motion picture film.) The control track signal is derived from the tonewheel pulse, which passes through a variable delay circuit before being formed into the sinusoidal signal, and thus bears a definite phase relationship to the video heads. (It should be noted that when the recorded control track signal is played back it will not appear to be sinusoidal but, because of the direct recording process instead of a linear recording process, it will exhibit a characteristic double-humped pattern.)

Superimposed upon the control track signal is a stable timing reference pulse designated the control-track frame pulse. This pulse is produced by a coincidence gate circuit which compares reference vertical and reference horizontal sync signals. The pulse occurs at a 30-cycle rate (25-cycle rate in International machines), and thus there will be one control track-frame pulse for every eight cycles of control track signal (every ten cycles in International machines). To meet SMPTE standards with regard to relative phasing between the control track signal and the control track-frame pulse, a variable delay is incorporated into the circuit which generates the control track signal. Thus, by maintaining a specific phase relationship, the control track-frame pulses provide physical locations on the tape (approximately every half inch) at which the tape may be cut and spliced without danger of picture roll-over (loss of vertical sync) during tape playback. Since the control track-frame pulse may be utilized as a guide for cutting tape during tape editing, it is sometimes referred to as an "edit" pulse.

The level of the composite control track/control track-frame pulse signal fed to the control track head is fairly critical. Therefore the simultaneous playback head is provided as a means of playing back the composite signal immediately after it has been recorded, so that the signal level may be observed on the CRO monitor and corrected if necessary. The composite signal may also be observed directly on the monitor as it is being recorded. This allows the operator to position the control track relative to the control track-frame pulse precisely and to obtain the correct pulse amplitude. In addition to these presentations on the CRO monitor, provision is made for observation of the matrixed motor drive sinusoidal signals as a means of checking the normal outputs which drive the capstan power amplifiers during the recording process.

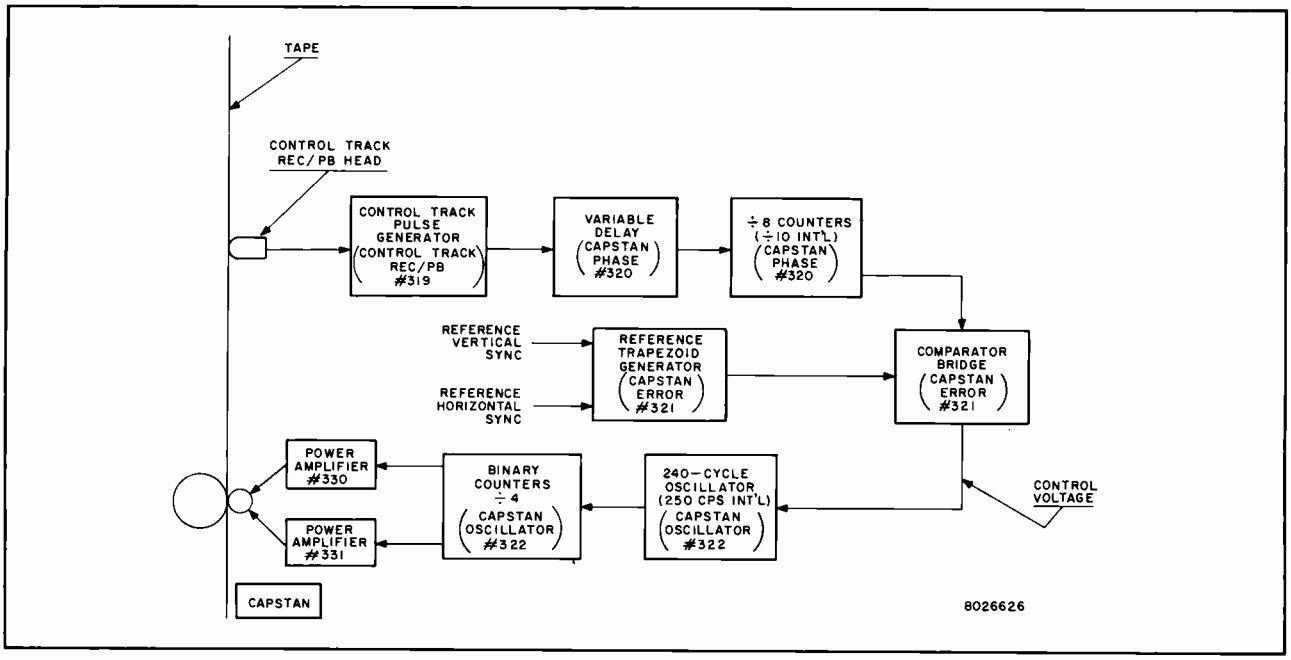


Figure 65—Capstan Servo System (Playback in Tonewheel Mode)

PLAY Mode

Tonewheel Servo Control

During tape playback in the tonewheel servo mode, the capstan servo controls the longitudinal tape speed and phasing so that the video heads track properly on the recorded video tracks. When playing back tape, the capstan motor speed is controlled by a local oscillator rather than by the tonewheel pulse as it is during the recording process. (See block diagram, figure 65, and functional diagram, figure 126.) The oscillator is "free-running" at a frequency of 240 cps; however, if the tape moves too slowly or too rapidly an error signal is developed which increases or decreases the oscillator frequency (and thus the capstan motor speed) to correct the tape speed. The 240-cycle output signal from the oscillator is divided-down and phase split by the binary counters and formed into the 60-cycle capstan motor drive signals, in exactly the same manner as is the tonewheel pulse during recording.

The error signal which modifies the local oscillator frequency to correct the tape speed is generated from the phase comparison of a pulse derived from the control track signal, which has been recorded on the tape, and a reference trapezoid waveform derived from local sync. The 240-cycle control track signal is played back from the tape by the control track REC/PB head, and is amplified, limited, and formed into a series of 240-cycle pulses. The 240-cycle pulses are then divided-down in frequency by a binary counter chain to obtain a series of 30-cycle pulses (25-cycle in International machines), which sample the slope of the reference trapezoid waveform to obtain the error signal. Local (reference) horizontal and vertical sync signals are combined in a coincidence gate circuit to form a pulse at the frame rate, and the reference pulse thus formed generates the reference trapezoid waveform. Therefore, as the tape speed increases or decreases, the control track pulse frequency follows this change and the error signal generated causes the capstan motor speed to decrease or increase until the divided-down frequency of the control track pulses coincides with that of the local stable timing reference pulse (i.e., the capstan motor speed is locked to the reference pulse frequency).

Provision is made for continuous manual control track phase variation over a very wide range. Manual phasing is accomplished by varying the C. T. PHASE control on the PLAY control panel, which in turn varies a delay inserted into the control track pulse path. The basic purpose of the manual delay is to provide a means of precisely centering the video heads over the recorded video tracks. In the tonewheel servo mode, the C. T. PHASE control may also be utilized in "slipping tracks" so that video head no. 1 will play back information from the video track containing vertical sync (which is normal operating procedure) or from any of the three remaining tracks. Provision is also made for manual control of the capstan motor speed during tape playback by interrupting the error signal fed to the 240-cycle local oscillator and inserting a d-c current which may be varied in magnitude by means of a control on the capstan error module front panel.

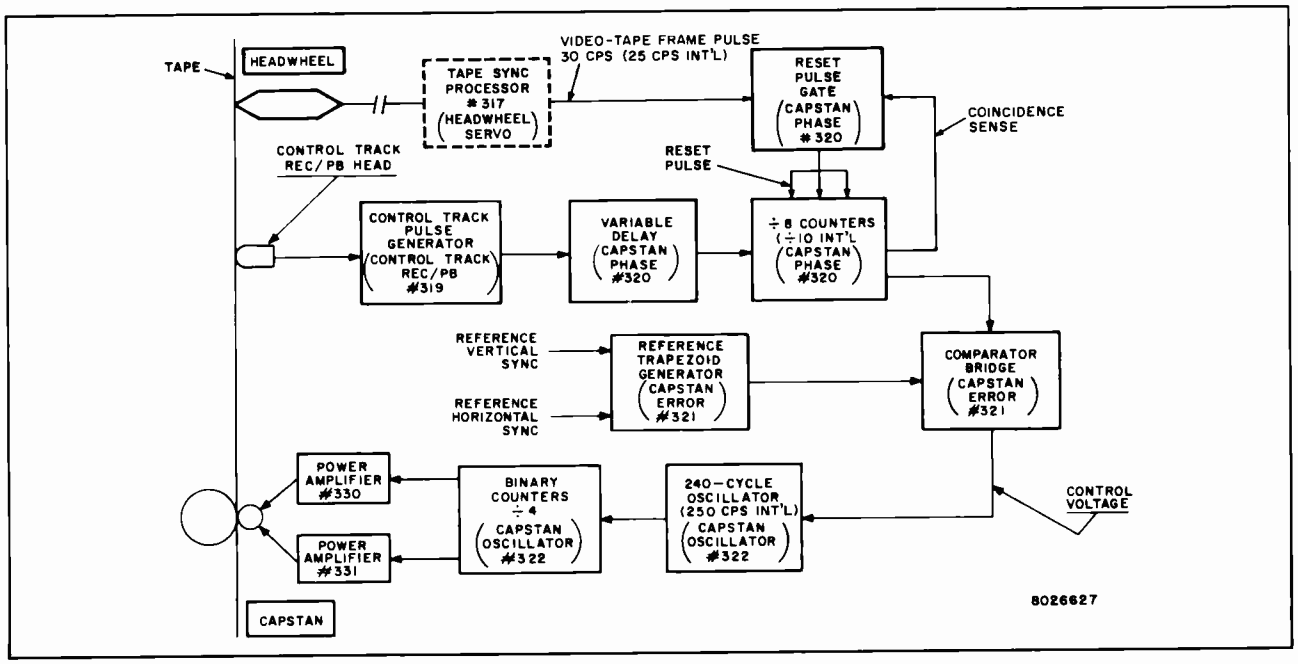


Figure 66—Capstan Servo System (Playback in Switchlock or Pixlock Mode)

Switchlock and Pixlock Servo Control

During tape playback in the tonewheel servo mode, the phasing of the control track pulse and a generated reference trapezoid waveform is such that there is only one chance in eight of beginning the binary count with tape and reference vertical sync signals aligned (one chance in ten on International machines). Therefore although the capstan servo will allow a clear, stable picture to be played back, there is no way of insuring that the phasing will be such that tape and reference vertical sync signals will be aligned each time a tape is played back. To insure sync alignment, and thus prevent picture roll-over when switching from tape to live camera, etc., the machine must be operated in switchlock (or pixlock) servo mode.

In the switchlock (or pixlock) servo mode, a "reset" pulse is developed which will automatically reset the binary counters and thus insure that the count begins with the control track pulse and reference trapezoid waveform phased so that tape and local reference vertical sync signals will be correctly aligned. (See block diagram, figure 66, and the functional diagram, figure 126.) The reset pulse is derived from the video-tape frame pulse which in turn is developed from the comparison of tape vertical and tape horizontal sync signals in a coincidence gate circuit. If the tape and reference vertical sync signals are aligned when the machine is switched to the switchlock servo mode of operation, the reset pulse will have no effect on the binary counter circuits. However, if the sync signals are not aligned, the reset pulse will re-set the binary counters and thus cause the machine to "shift tracks" until sync alignment is attained. The shifting of tracks is designated "coarse vertical framing" and results in approximate alignment of tape and reference vertical sync. More precise vertical framing is not possible (nor necessary) during switchlock servo operation however, because there is no compensation for errors of placement of vertical sync in the recorded pattern on the tape. To compensate for these errors, the machine must be operated in the pixlock servo mode and the corrections are then actually made by the headwheel servo system.

During tape playback in switchlock or pixlock servo mode, the C.T. PHASE control may be utilized in precisely centering the video heads over the recorded video tracks as it is during playback in the tonewheel servo mode. However, in the switchlock or pixlock servo mode it is not possible to use the C.T. PHASE control to "slip tracks" because proper switchlock operation requires that video head no. 1 play back the track containing vertical sync (normally track no. 1).

> IMPORTANT: To play back tape in the switchlock or pixlock mode of servo operation, the servo reference must be external (local sync) and not line. (I.e., the SERVO REF pushbutton on the PLAY control panel must be pressed for EXT operation.) This is because horizontal sync, required by the switchlock and pixlock circuits, is not present when line servo reference is utilized.

CAPSTAN SERVO SETUP PROCEDURE

The setup procedure outlined below is divided into sections which specify adjustments for each individual module. To facilitate the overall system adjustments, the procedure should be followed in the modular order presented. All waveforms and voltages specified may be monitored directly on the machine, and therefore no external test equipment is necessary. Alternate adjustment procedures are presented at the end of each module circuit description, and may in some cases prove to be more convenient.

Capstan Oscillator (no. 322)

ϕ_1 and ϕ_2 Gain

1. Place machine in SETUP mode.

2. Press CM1 pushbutton (located above the guide servo module, no. 221), and vary AMPL 1 adjustment to obtain a reading of 110 volts on the multimeter (located below the picture monitor).

3. Press CM2 pushbutton, and vary AMPL 2 adjustment to obtain a reading of 110 volts on the multimeter.

Oscillator Frequency and Phase

1. Play back a "standard" test tape.

2. Rotate C.T. PHASE control (on PLAY control panel) to "0" position, and press CAP SERVO pushbutton on CRO monitor switcher.

3. With self-release button on module front panel depressed, vary OSC FREQ control to stop relative motion between pip and trapezoid waveform, as observed on CRO monitor.

4. Release button (capstan should now "lock") and fine adjust the OSC FREQ control so that the pip is located 40% up from the bottom of the trapezoid slope as shown in figure 67.

NOTE: The pip should not be located half-way up the trapezoid slope, but 40% as specified in step 4. This assures maximum oscillator "lock-in" range.

Capstan Error (no. 321)

Tracking Zero Set

1. Play back a "standard" test tape.

2. Rotate function selector switch on tape sync processor module (no. 317) to TW position, and head select switch on reference generator module (no. 312) to "1" position.

3. Press SW OUT pushbutton on CRO monitor switcher.

4. Observing the CRO monitor, vary the C.T. PHASE control (on PLAY control panel) slightly to center head no. 1 on track no. 1, as indicated on the CRO monitor by maximum amplitude of the rf band containing vertical sync.

NOTE: To verify that head no. 1 is centered on track no. 1, a sharp increase in amplitude of the rf band containing vertical sync should be noted when the CH ID button on playback amplifier no. 1 (module no. 215) is pressed.

5. Slowly rotate the C.T. PHASE control toward "0" position while simultaneously varying the TRACKING ZERO SET adjustment so that head no. 1 remains centered on track no. 1.

6. When the C.T. PHASE control has reached "0" position, peak the rf band amplitude with the TRACKING ZERO SET adjustment.

Control Track Record/Playback (no. 319)

Control Track Record Current

1. Place blank tape on machine and operate machine in RECORD mode.

2. Press CT PB pushbutton on CRO monitor switcher.

3. Observe waveform on CRO monitor and vary CT RECORD adjustment to obtain a level which just produces "verge of tape saturation", or characteristic double-humped waveform, as shown in figure 68.

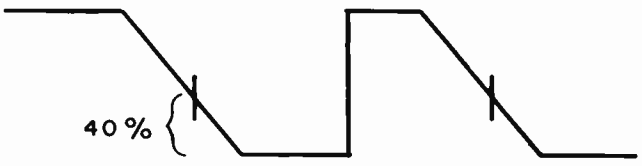


Figure 67—Correct Location of Pip on Trapezoid Slope

Figure 68—Correct Control Track Playback Waveform

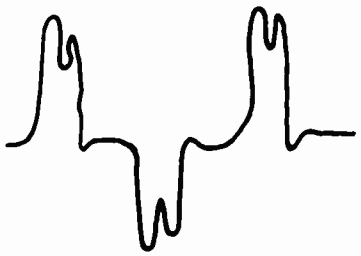


Figure 69—Excessive Control Track Record Current

Figure 70—Insufficient Control Track Record Current

NOTE: Excessive record current produces a spiked waveform as shown in figure 69 and will cause objectionable crosstalk between the control track signal and cue audio, thereby reducing the cue channel signal-to-noise ratio. Conversely, too little record current produces the pattern shown in figure 70 and can cause unreliable or no servo "lock-up"

Control Track Phase

1. Place machine in SETUP mode.

2. Press CT REC pushbutton on CRO monitor switcher.

3. Observe waveform on CRO monitor and rotate FRAME PULSE RECORD adjustment in a clockwise direction until a very small positive-going pip is observed on the sinusoidal waveform.

4. Vary RECORD CTϕ adjustment to center the pip in the negative-going portion of the sinusoidal waveform as shown in figure 71.

Frame Pulse Amplitude

With machine in SETUP mode and the CT REC pushbutton on the CRO monitor switcher depressed, vary the FRAME PULSE RECORD adjustment to obtain a frame pulse amplitude which is $1\frac{1}{2}$ times the peak-to-peak amplitude of the sine wave (figure 72).

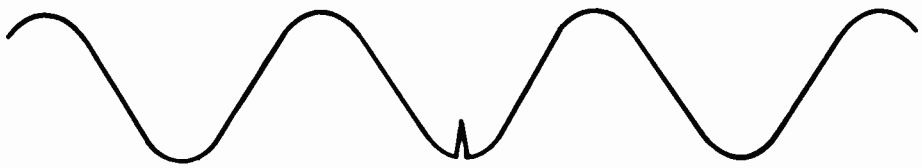


Figure 71—Control Track Phase Adjustment Waveform

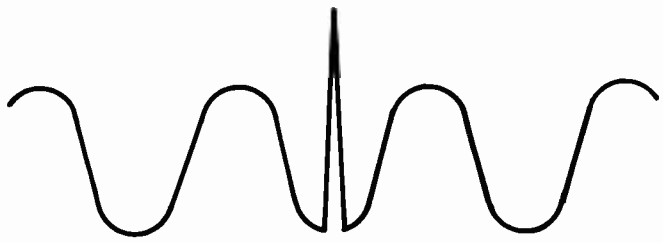


Figure 72—Frame Pulse Amplitude Adjustment Waveform

MODULE CIRCUIT ANALYSES

In the following analyses of the individual modules which are contained in the capstan servo system, timing references pertain to domestic standards; i.e., a 15,750 cps horizontal rate (525-line) and a 60-cycle field rate. A special capstan phase module (no. 320) will be utilized in the International machines to accommodate International line standards and a 50-cycle field rate. The description of this module is presented separately, following the domestic module description. The remaining modules in the capstan servo system contain circuitry which allows them to operate efficiently in either domestic or International machines.

Partial schematic diagrams are intended to show only the area under discussion. For a complete schematic diagram refer to the *TR-22 TV Tape Recorder Diagram Manual,* IB-31616. A functional diagram of the capstan servo system (figure 126) will be found at the rear of this instruction book. This diagram is provided as an aid in obtaining an overall conception of the function of the circuits which compose the modular portion of the capstan servo system.

CONTROL TRACK RECORD/PLAYBACK MODULE

Circuit Description

General

The control track REC/PB module (no. 319) has two basic functions in the capstan servo subsystem. In the RECORD mode of tape recorder operation, the module circuitry converts a 240-cycle tonewheel pulse from the headwheel servo subsystem into a 240-cycle sine wave signal whose phase is variable with respect to that of the tonewheel pulse. This signal is the control track signal, and is recorded on the tape by the control track head located on the headwheel panel. In the PLAY mode of operation, different circuits in the module receive the control track signal from the tape and convert it into a series of narrow rectangular pulses having a definite phase relationship with the tonewheel pulse. These pulses are used to trigger a chain of binary counters in the capstan phase module

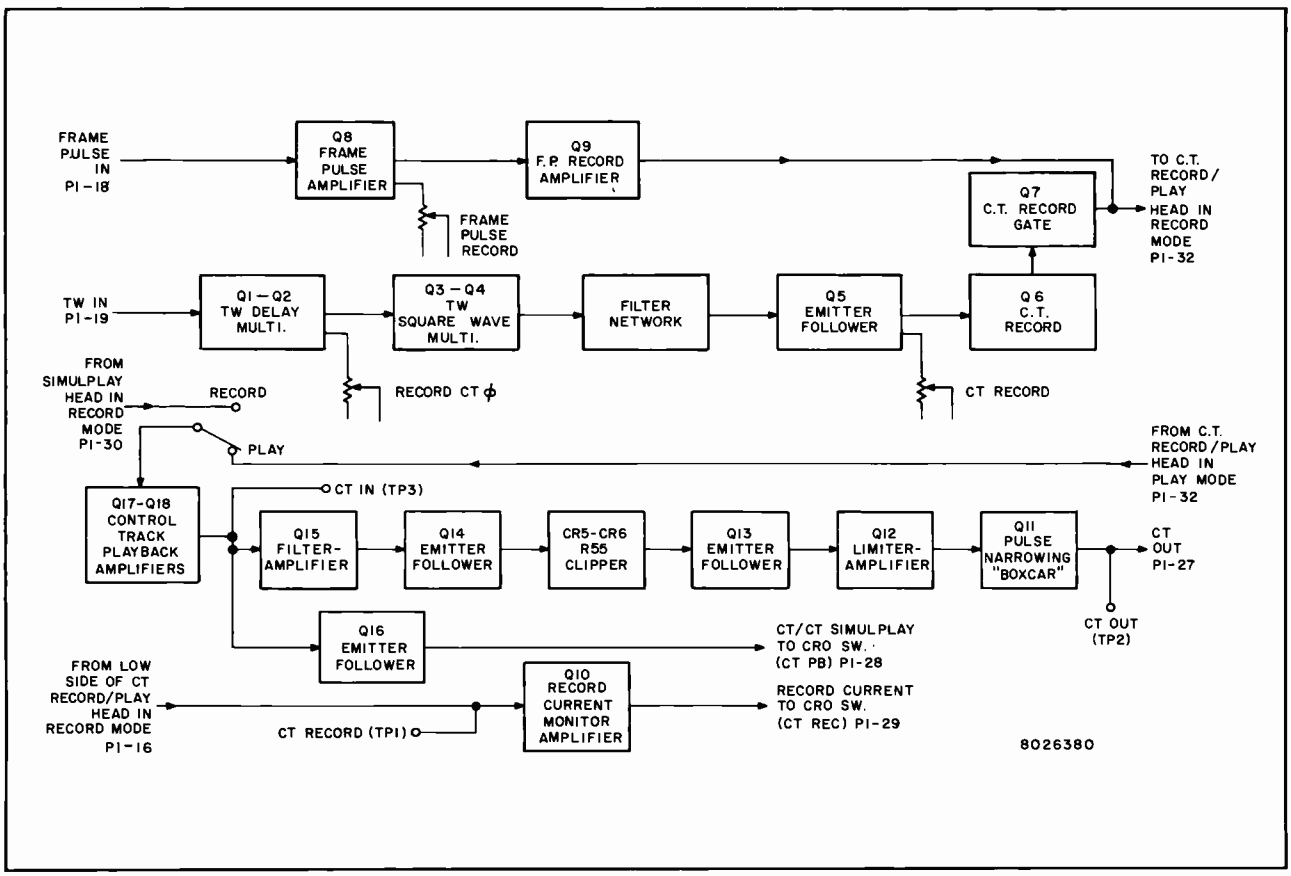


Figure 73—Control Track REC/PB Module Block Diagram

(no. 320). Portions of the playback amplifier circuits are also used when the machine is operated in the RECORD mode. In this case the control track signal is picked up from the tape by the control track simultaneous playback head, amplified, and fed to the CRO monitor to make certain that the proper signal is being recorded.

Circuits are also provided in the module for amplifying the frame pulse (which is developed in the capstan error module, no. 321) and combining it with the control track signal; and for supplying the CRO monitor switcher with the control track signal for monitoring purposes on the CRO monitor during tape playback and recording (simultaneous playback).

The choice of module function is selected by relay K1 (see block diagram, figure 73) which is deenergized when the machine is operated in the PLAY mode, and energized when operated in the RECORD mode.

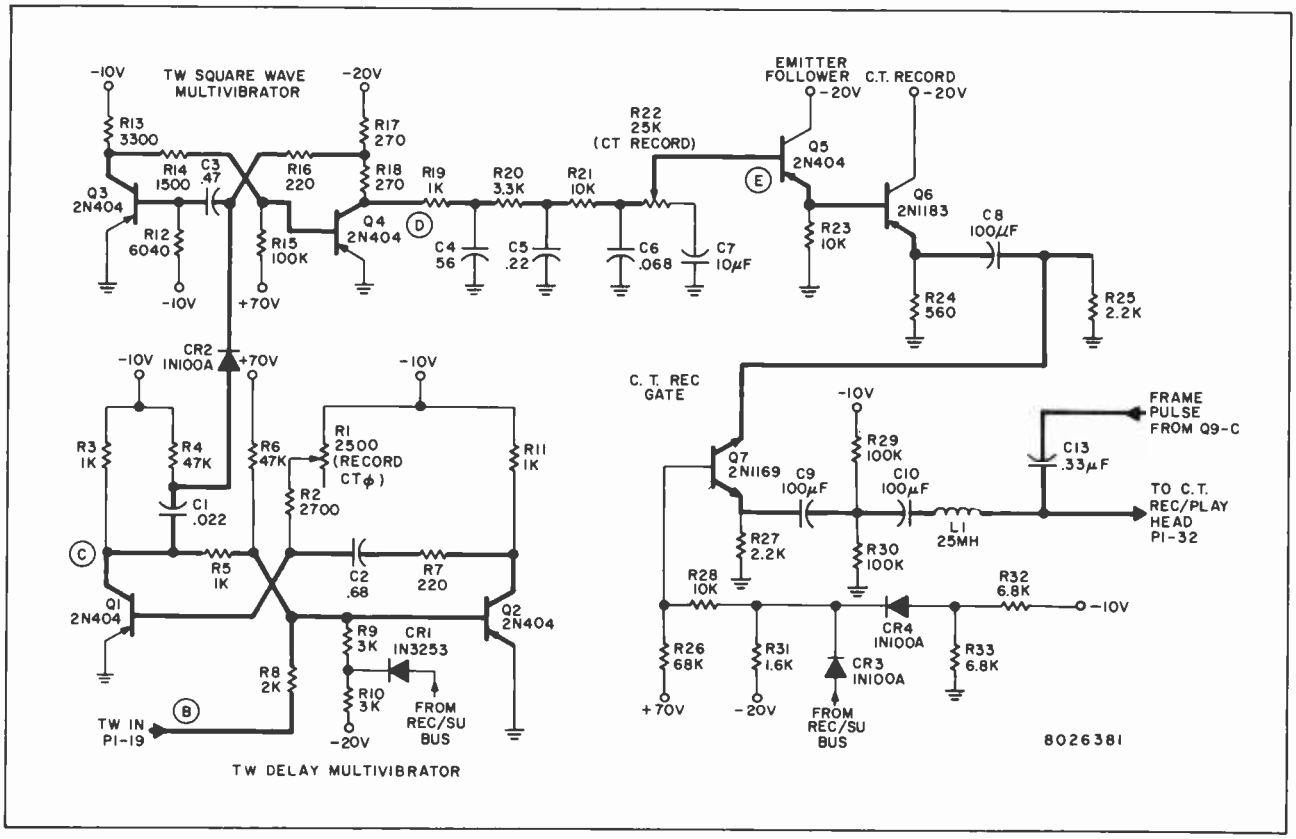
Control Track Sine Wave Generator

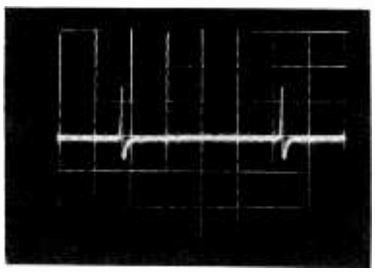
The control track sine wave generator circuit, which is utilized only when the machine is operating in the RECORD mode, is shown in figure 74. The input to the circuit is the tonewheel pulse (figure 74A), which is amplified and shaped in the tonewheel processor module of the headwheel servo subsystem before being fed to the control track REC/PB module at pin 19 of plug P1 (figure 74B). This pulse is then used in triggering the one-shot monostable delay multivibrator Q1-Q2. In the delay multivibrator stable state, transistor Q1 is conducting and transistor Q2 is cut off. When the negative-going tonewheel pulse appears at the base of transistor Q2, the transistor is driven into conduction and the multivibrator goes into its unstable state for a length of time which depends upon the time constant developed by capacitor C2 charging through resistor R2 and potentiometer R1. The resultant output at the collector of transistor Q1 then, is a negative-going pulse whose width is determined by the time constant of C2, R1, and R2. Since the positive-going trailing edge of the pulse output is used to trigger square wave multivibrator Q3-Q4, the generation of the square wave may be delayed over a range of approximately ± 600 microseconds with respect to the tonewheel pulse by adjusting potentiometer R1 (RECORD CTϕ) and thus varying the time constant. (The reason for providing this variable delay is explained below in the discussion on the frame pulse amplifier stages, and the method of correctly adjusting potentiometer R1 is outlined in the *Adjustment* section.)

In the RECORD or SETUP mode, the REC/SU bus is at ground potential and diode CR1 is forward biased. This places the junction of resistors R9 and R10 at ground potential, and the delay multivibrator functions normally. During tape playback however, the REC/SU bus is at -26 volts dc and the diode is cut off. In this case, transistor Q2 is saturated due to the negative potential applied to its base through resistors R9, R10 and the multivibrator is disabled, thus rendering the remaining sine wave generating circuits inoperative. The function of diode CR1 then, is to disable the delay multivibrator when the machine is operating in the PLAY mode. This precaution is taken to prevent any possibility of crosstalk interference with the high gain playback amplifier circuit during tape playback.

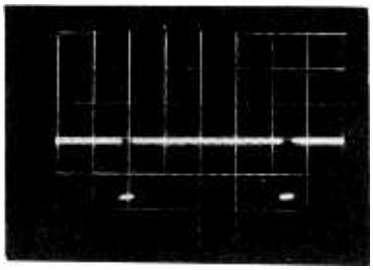
The negative-going pulse output at the collector of transistor Q1 (figure 74C) is differentiated by capacitor C1 and resistor R4, and the positive-going spike resulting from the differentiation is fed through diode CR2 to the base of transistor Q3. Transistors Q3 and Q4 form a conventional one-shot monostable multivibrator, whose purpose is to generate a 240-cycle square wave. In the multivibrator stable state, transistor Q3 is biased into saturation while transistor Q4 is biased at cut-off. The positive-going spike fed to the base of transistor Q3 cuts the transistor off, thus initiating the multivibrator action. Since the positive-going spike corresponds to the positive-going trailing (delayed) edge of the pulse output from delay multivibrator Q1-Q2, the generation of the 240-cycle square wave will be delayed by a finite time interval which is dependent upon the setting of the RECORD CTϕ potentiometer.

The 240-cycle square wave output from transistor Q4 (figure 74D) is fed to a three-section low-pass filter network which converts the square wave into a relatively pure sine wave. The filter sections are impedance scaled to obtain a degree of isolation between each section, thereby reducing the loading effect which each resistance-capacitance section presents to the preceding one. Capacitor C7 (10 μfd) acts as an a-c ground; thus the sine wave is developed across potentiometer R22 (CT RECORD) and is fed to the base of emitter follower transistor Q5 (figure 74E). (Potentiometer R22 may be adjusted to vary the

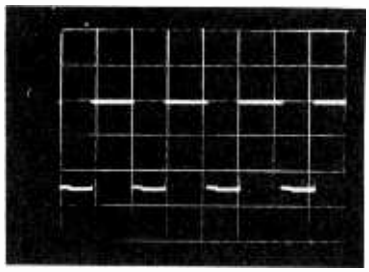




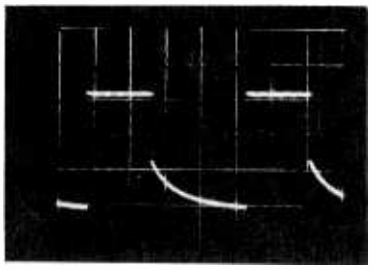
A. Tonewheel Pulse (TW IN Test Point on TW PROC Module, no. 313), 0.5v/cm.



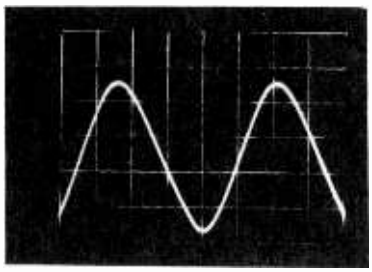
B. TW IN (P1-19), 5v/cm.



C. Q1 collector, 2v/cm. (2 msec/cm)



D. Q4 collector, 5v/cm.



E. Q5 base, 0.5v/cm.

Machine in RECORD or SETUP mode. All sweep times 1 msec/cm, unless otherwise noted.

Figure 74—Control Track Sine Wave Generator

amplitude of the sine wave signal, as explained in the *Adjustment* section.) Transistors Q5 and Q6 are cascaded emitter followers, and their purpose is to reduce the high impedance output of the filter network to an impedance which is low enough to provide sufficient current gain to drive the control track record/playback head.

Gating transistor Q7 is a bilateral transistor (i.e., either electrode may act as emitter or collector), and is utilized in the control track record path as an additional precaution to prevent crosstalk into the playback amplifier circuit during the PLAY mode of operation. As mentioned previously, the REC/SU bus is at ground potential when the machine is operated in the RECORD or SETUP mode and at −26 volts dc when operated in the PLAY mode. In the RECORD mode then, diode CR3 is forward biased and the junction of the diode and resistor R28 is essentially at ground potential. The voltage drop across resistor R28 is applied to the base of gating transistor Q7 as a positive bias voltage which causes the transistor to saturate and thereby present a low impedance path to the sine wave signal. In the PLAY mode, diode CR3 is biased off and the base of transistor Q7 then goes negative, thus cutting the transistor off and preventing any crosstalk or other spurious signals from passing through to the playback amplifier circuit during tape playback. (The purpose of diode CR4 is to make certain diode CR3 is disconnected during the PLAY mode of operation, thereby eliminating any loading effect on the REC/SU bus.)

The 240-cycle sine wave signal passed by gating transistor Q7 is coupled through capacitors C9, C10 and coil L1 to the junction of coil L1 and capacitor C13 (figure 74F). (Two coupling capacitors connected back-to-back are used to insure definite electrolyte polarization and thereby greatly lengthen capacitor life.) The 240-cycle sine wave at the junction of L1 and C13 is the control track signal, and is combined with the frame pulse (as explained below in the frame pulse amplifier discussion) before being fed through pin 32 of plug P1 to the control track record/playback head.

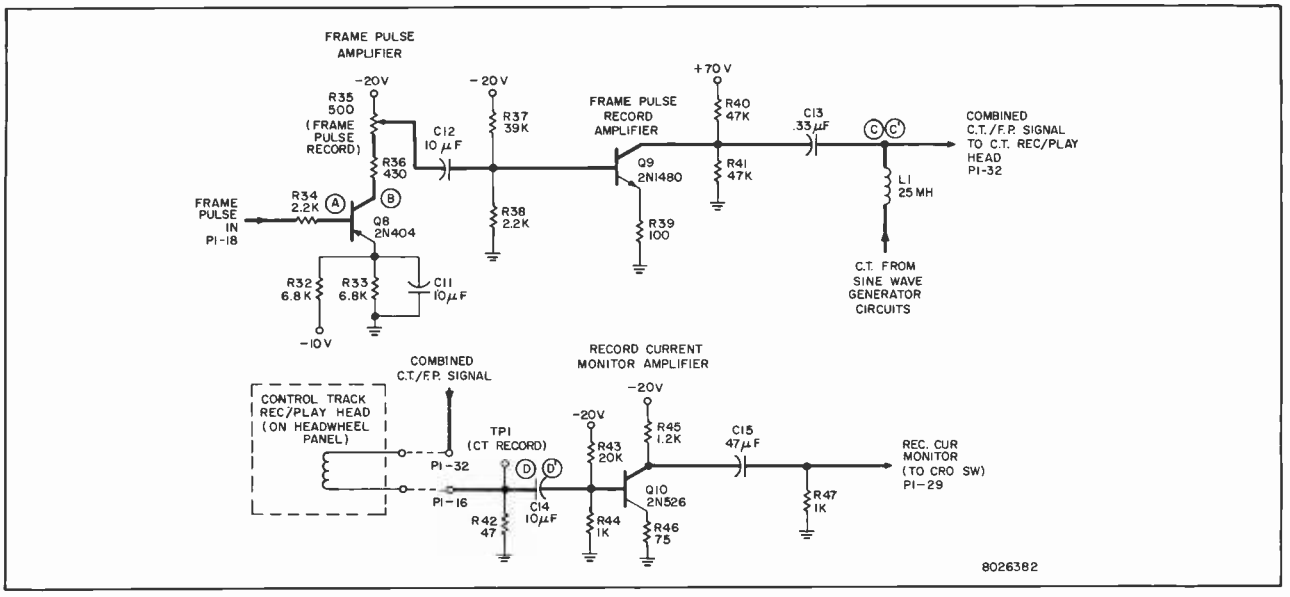
Frame Pulse and Record Current Monitor Amplifiers

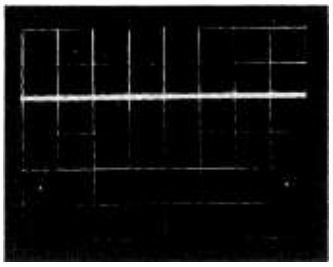
The frame pulse, developed in the capstan error module (no. 321), is fed to the control track REC/PB module at pin 18 of plug P1 as a narrow negative-going pulse occurring at a 30-cycle rate (25-cycle rate in International machines). From pin 18, the pulse is fed to the base of frame pulse amplifier transistor Q8 through current limiting resistor R34 (figure 75A). Transistor Q8, normally cut off by the negative bias voltage applied to its emitter, is driven into saturation by the negative-going frame pulse fed to its base. This results in a positive-going pulse at the collector of transistor Q8 (figure 75B), which is then coupled to the base of frame pulse record amplifier transistor Q9. Potentiometer R35 (FRAME PULSE RECORD), in the collector circuit of transistor Q8, is provided as a means of varying the amplitude of the pulse applied to the base of transistor Q9. This adjustment is important in obtaining the proper amplitude relationship between the control track signal and frame pulse (see *Adjustments*).

Transistor Q9 is normally cut off by the negative bias voltage applied to its base, and the positive-going pulses from the center-arm of potentiometer R35 drive the transistor into saturation. The pulse at the collector of transistor Q9 is then negative-going, and is fed to the junction of capacitor C13 and coil L1. Here the 30-cycle frame pulse is combined with the 240-cycle control track sine wave (figure 75C) and, because of their relative frequencies, there will be one frame pulse for every eight cycles of control track signal. (In International machines the frame pulse rate is 25 cps; therefore there will be one frame pulse for every ten cycles of control track signal, as shown in figure 75C′.)

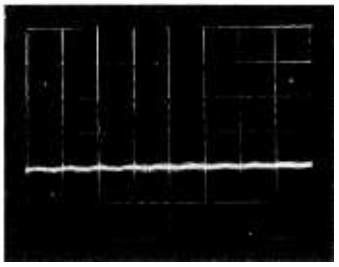
In the RECORD mode of operation relay K1 is energized, and the combined signal is fed from the junction of capacitor C13 and coil L1 through pin 32 of plug P1 to the control track record/playback head. The inductive reactance of coil L1 is such that it presents a low impedance path to the 240-cycle control track sine wave signal, thus allowing the signal to pass, while at the same time it presents a high impedance to the narrow 30-cycle frame pulse, thus preventing the pulse from being shunted to ground by the very low output impedance of the control track record transistor Q6.

The low side of the control track head is returned to ground in the control track REC/PB module through pin 16 of plug P1 and resistor R42, a 47 ohm current sampling resistor. In the RECORD mode, the combined frame pulse and control track signal which appears across sampling resistor R42 is applied to the record current monitor amplifier transistor Q10, and may be observed on the CRO monitor or at test point TP1 (CT RECORD). Figure 75D shows the combined signal appearing at test point TP1 on domestic machines (240-cycle control track rate), while figure 75D′ shows the signal appearing at TP1 on International machines (250-cycle control track rate).

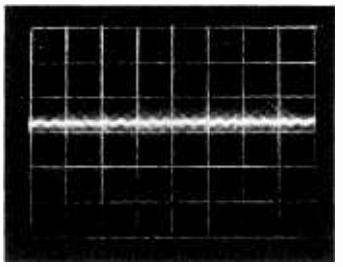




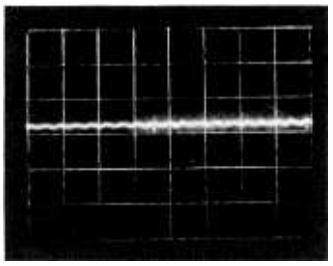
A. Q8 base, 2v/cm.



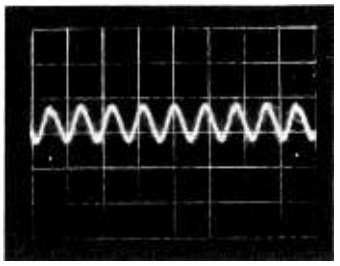
B. Q8 collector, 5v/cm.



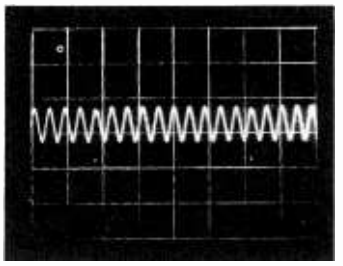
C. Junction C13 and L1, 240-cycle CT, 20v/cm. (10 msec/cm)



C'. Junction C13 and L1, 250-cycle CT, 20v/cm. (10 msec/cm)



D. TP1 (CT RECORD), 240-cycle CT, 0.5v/cm.

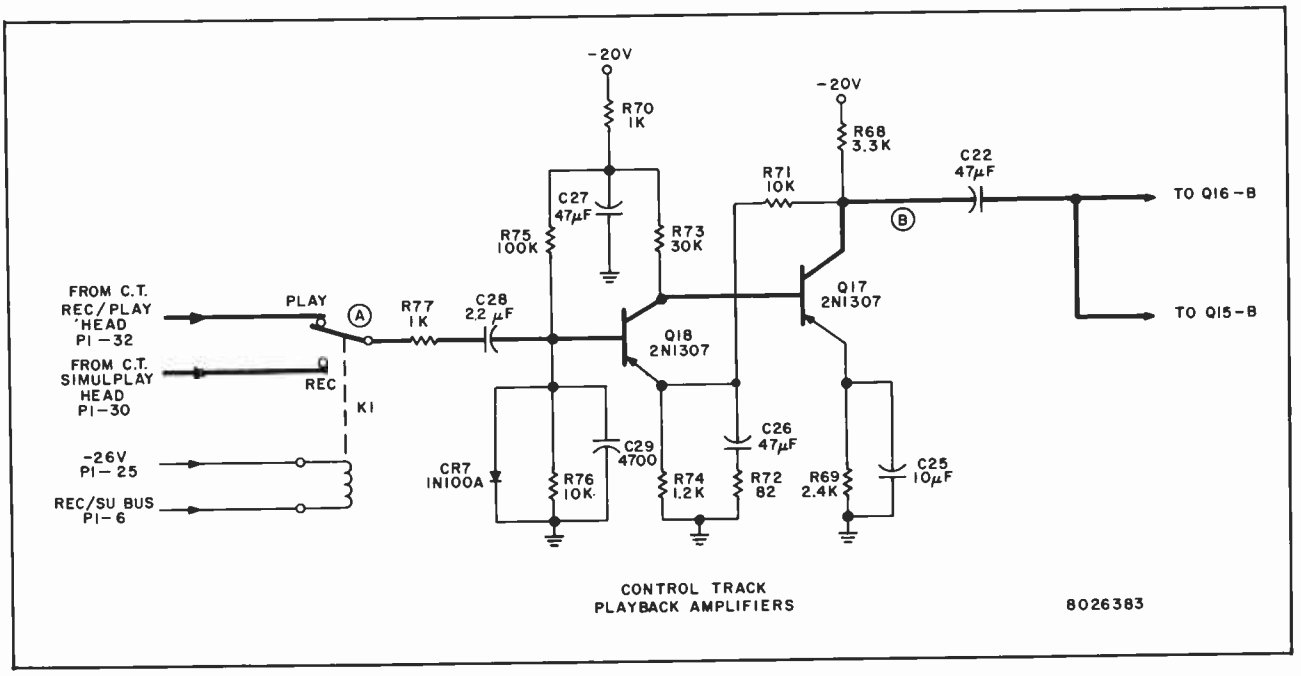


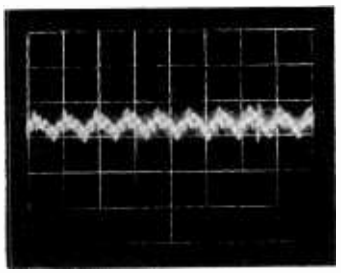
D'. TP1 (CT RECORD), 250-cycle CT, 0.5v/cm. (10 msec/cm)

Machine in PLAY mode. All sweep times 5 msec/cm, unless otherwise noted.

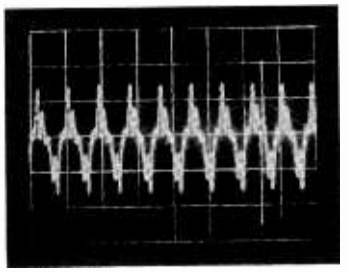
Figure 75—Frame Pulse and Record Current Amplifiers

Transistor Q10 amplifies the signal appearing across resistor R42, and the output at the collector of Q10 is fed through pin 29 of plug P1 to the CRO monitor switcher. Thus, in the RECORD mode, the combined frame pulse and control track signal may be observed on the CRO monitor by pressing the CT REC push-button on the CRO monitor switcher. *Note that the waveform seen on the CRO monitor is inverted with respect to the waveform observed at test point TP1, due to the monitor amplifier transistor Q10. The combined frame pulse and control track signal viewed at test point TP1 should correspond in phase and relative amplitudes to the SMPTE standard combined waveform.* (Keeping the waveform inversion in mind, the CRO monitor may be used in setting up the SMPTE standard RECORD conditions as described in the *Adjustments* section.)





A. Junction K1 and R77, .005v/cm.



B. Q17 collector, 0.1v/cm.

Machine in PLAY mode. All sweep times 5 msec/cm.

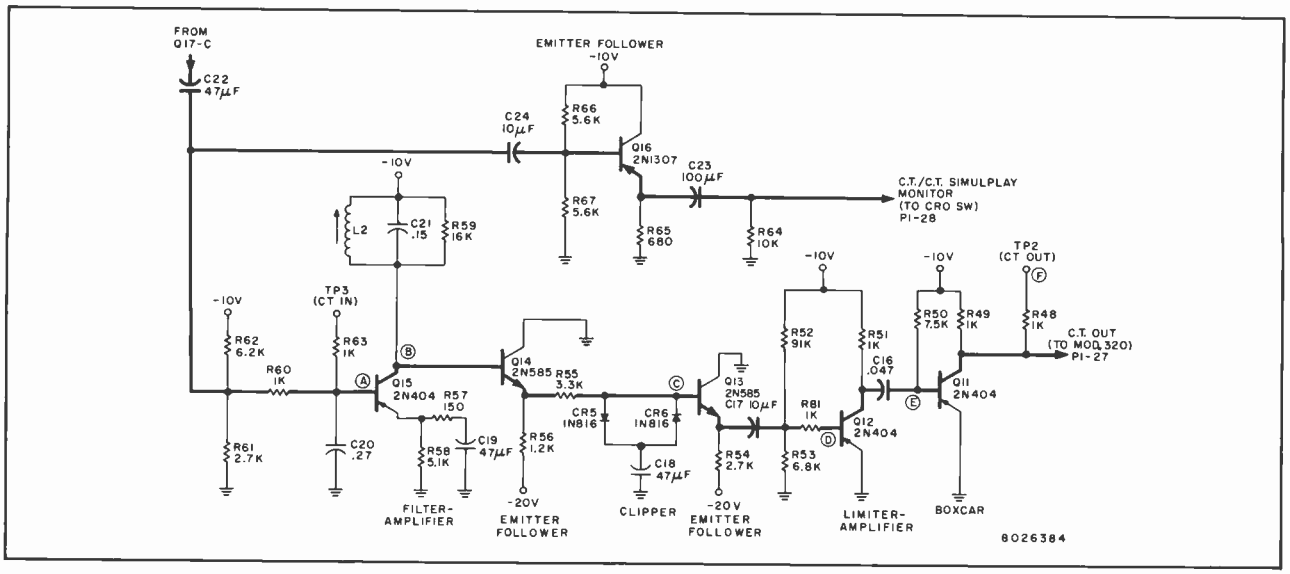
Figure 76—Control Track Playback Amplifiers

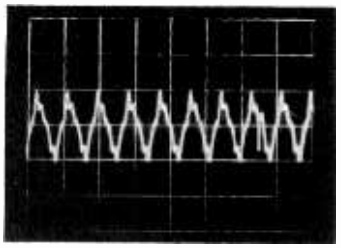
Control Track Playback Amplifier

In the PLAY mode of tape recorder operation relay K1 is deenergized, and the combined control track and frame pulse signal is fed from the control track record/playback head to the control track playback amplifier circuit (figure 76), through pins 32 and 16 of plug P1. A protective circuit consisting of resistor R77 and diode CR7 eliminates the possibility of any damage to transistor Q18 which may be caused by switching transients during the relay switching interval. Capacitor C29 (4700 $\mu\mu$fd) and resistor R77 (1000 ohms) form a low-pass filter network which rolls off any extraneous high frequency signals that may be picked up in the control track cabling, such as spurious rf signals, high frequency crosstalk, etc.

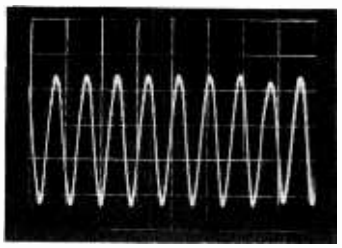
In the RECORD mode, the combined control track and frame pulse signal is picked up from the tape by the control track simultaneous playback head (located on the tape transport panel) and is fed to the control track REC/PB module at pins 30 and 14 of plug P1 (pin 14 is grounded in the module). The signal is then passed through the roll-off and protective networks mentioned in the paragraph above, and on to the base of amplifier transistor Q18 (figure 76A).

Transistors Q17 and Q18 form a gain-stabilized feedback pair which amplify the control track signal to approximately 0.3 volt peak-to-peak (figure 76B) before it is fed simultaneously to emitter follower transistor Q16 and filter-amplifier transistor Q15. Emitter follower transistor Q16 provides the low impedance required to drive the 75-ohm input to the CRO monitor, and the control track signal at the emitter of Q16 is fed to the CRO monitor switcher from pin 28 of plug P1. Thus the control track signal, as it is recorded on the tape, may be observed on the CRO monitor in either PLAY or RECORD (simultaneous playback) mode by pressing the CT PB pushbutton on the CRO monitor switcher.

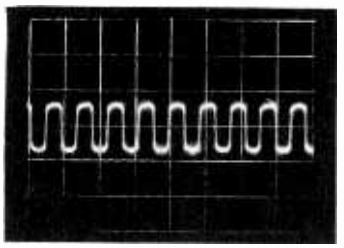




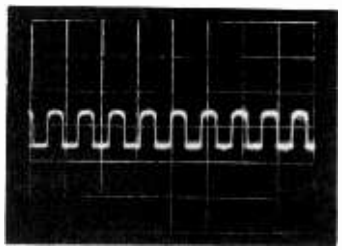
A. Q15 base, 0.1v/cm.



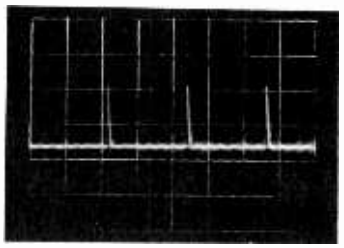
B. Q15 collector, 2v/cm.



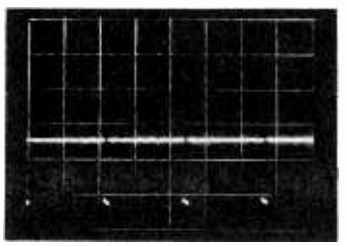
C. Q13 base, 1v/cm.



D. Q12 base, 1v/cm.



E. Q11 base, 5v/cm. (2 msec/cm)



F. TP2 (CT OUT), 5v/cm. (2 msec/cm)

Machine in PLAY mode. All sweep times 5 msec/cm, unless otherwise noted.

Figure 77—Control Track Pulse Generator

Control Track Pulse Generator

The control track pulse generator circuit shown in figure 77 is utilized only when the machine is operated in the PLAY mode, and its purpose is to convert the control track signal picked up from the tape by the control track head into a series of rectangular pulses which are used in the capstan phase module (no. 320).

The control track signal fed from transistor Q17 to the base of filter-amplifier transistor Q15 may be observed at test point TP3 (CT IN) and is shown in figure 77A. Capacitor C20 (.27 μfd) and resistor R60 (1000 ohms) form a second low-pass filter network which reduces the harmonic content of the signal applied to the base of Q15. Transistor Q15 is a tuned amplifier, and the tuned circuit consisting of capacitor C21 and variable inductor L2 in its collector circuit serves a two-fold purpose due to its action as both a filter and a "ringing" circuit. As a filter circuit, its function is to further reduce the harmonic content of the signal fed to the base of Q15 and thus produce a relatively pure sine wave signal at its collector. As a ringing circuit, its function is to continue to furnish a signal to the pulse forming circuits whenever a momentary loss in control track signal occurs (caused by dropouts, bad splices, etc.) and thus prevent the servo from falling out of lock if the control track signal is lost for several cycles.

Resistor R59 is connected in parallel with the tuned circuit to lower the circuit "Q", so that the circuit is broadly resonant at 240 cps and thus will easily pass both the 240-cycle signal and the 250-cycle signal used in International machines. (Inductor L2 is factory tuned for 240/250 cps and should not normally require field adjustment. However, if either the inductor or capacitor C21 are replaced, re-tuning will be necessary and the procedure given in the *Adjustment* section should be followed.)

The signal at the collector of transistor Q15 is an approximate sine wave occurring at a 240-cycle rate (250 cps in International machines), and has a nominal amplitude of 7.5 volts peak-to-peak (figure 77B). This signal is fed to emitter follower transistor Q14 which drives the symmetrical clipper stage consisting of diodes CR5, CR6 and resistor R55. Diodes CR5 and CR6 are silicon, and each has a forward voltage drop of approximately 0.6 volt; thus the incoming sine wave is clipped to an amplitude of approximately 1.2 volts peak-to-peak (figure 77C).

The clipped 240-cycle signal is fed to emitter follower transistor Q13 which drives the limiter-amplifier transistor Q12 (figure 77D). Limiting action takes place in the base circuit of transistor Q12, and the amplified pulse output at the collector of Q12 is fed to the base of transistor Q11 (figure 77E). Transistor Q11 operates as a pulse-narrowing "boxcar" circuit, and produces a series of narrow, negative-going pulses at its collector. These pulses occur at a 240/250-cycle rate and are fed through pin 27 of plug P1 to the capstan phase module (no. 320) where they are used to drive a chain of binary counters. Test point TP2 (CT OUT) is provided for convenience in observing the output control track pulses, which appear as shown in figure 77F.

Adjustments

The three potentiometer adjustments described below are not routine operation adjustments, but should be checked at regular intervals. The variable inductor (L2) in the collector circuit of transistor Q15 has been properly tuned at the factory for 240/250-cycle operation and should not require any further adjustment; however, if either the inductor or capacitor C21 in the tuned circuit are replaced, re-tuning is necessary and one of the two procedures outlined below should be followed.

Test equipment required for tuning inductor L2 consists of an oscilloscope such as the *Tektronix Type 535A* or equivalent and, with the second method, a well calibrated audio oscillator such as the *Hewlett-Packard Type 200CD* or equivalent.

Control Track Record

1. Thread blank tape on machine, and place machine in RECORD mode of operation.

2. Press CT PB pushbutton on CRO monitor switcher.

3. While observing waveform on CRO monitor, adjust CT RECORD potentiometer on module front panel for a level which just produces "verge of tape saturation" or the characteristic "double-humped" pattern shown in figure 78A.

NOTE: Excessive record current produces a spiked pattern, as shown in figure 78B, and will cause excessive crosstalk of control track into cue audio, thereby reducing the cue channel signal-to-noise ratio. On the other hand, too little record current produces the pattern shown in figure 78C, and can cause unreliable or no servo "lock-up".

Control Track Phase

1. Place machine in SETUP mode, and press CT REC pushbutton on CRO monitor switcher.

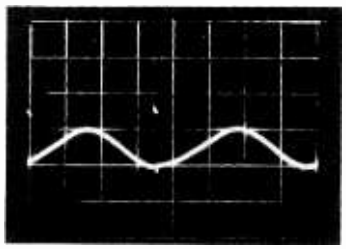
2. While observing waveform on CRO monitor, adjust the FRAME PULSE RECORD potentiometer to obtain a very small positive-going pip.

NOTE: Reducing the frame pulse amplitude while performing this adjustment will make it possible to adjust the RECORD CTϕ potentiometer much more accurately.

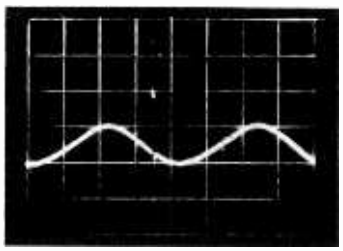
A. Normal CT RECORD current. **B. Excessive CT RECORD current.** **C. Insufficient CT RECORD current.**

Machine in RECORD mode; waveforms obtained at Q17 collector. Sweep times 2 msec/cm; amplitudes 0.1v/cm.

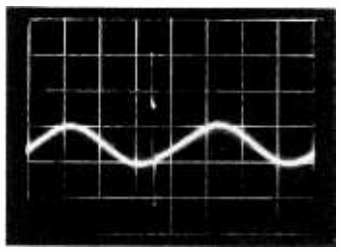
Figure 78—Waveforms Indicating Correct and Incorrect Settings of CT RECORD Adjustment



A. RECORD CTØ potentiometer correctly adjusted.



B. RECORD CTØ potentiometer rotated fully clockwise.



C. RECORD CTØ potentiometer rotated fully counterclockwise.

Machine in SETUP mode; waveforms obtained at TP1 (CT RECORD). Sweep times 1 msec/cm; amplitudes 0.5v/cm.

Figure 79—Waveforms Indicating Correct Setting and Range of RECORD CTϕ Adjustment

3. Adjust the RECORD CTϕ potentiometer so that the pip is exactly centered in the negative half of the sine wave, as shown in figure 79A. (The composite control track/frame pulse waveform is shown in figure 79B with the RECORD CTϕ potentiometer rotated fully clockwise, and in figure 79C with the potentiometer rotated fully counterclockwise.)

Frame Pulse Record

1. Place machine in SETUP mode, and press CT REC pushbutton on CRO monitor switcher.

2. While observing waveform on CRO monitor, adjust FRAME PULSE RECORD potentiometer to obtain a frame pulse amplitude equal to $1\frac{1}{2}$ times the peak-to-peak amplitude of the control track sine wave. See figure 79.

NOTE: The waveform observed on the CRO monitor (figure 79) is inverted relative to the waveform observed at the CT RECORD test point (figure 75D).

Tuned Circuit (Inductor L2)

Either method of tuning inductor L2 presented below will give sufficiently accurate results. *When using the first method, it is very important that the machine be properly locked while recording and playing back the tape.*

1. Record several minutes of tape on a machine which is operating normally. (The machine should be locked to the local servo reference; preferably to the local sync generator.)

2. Make sure that the headwheel is locked. (Press CT REC pushbutton on CRO monitor switcher and observe waveform on the CRO monitor. The frame pulse and control track signals should be locked.)

3. Re-wind the recorded portion of the tape, and place the module on a module extender.

4. Attach low capacitance oscilloscope probe to the collector of transistor Q15 and play back tape while observing the waveform on the oscilloscope.

5. Tune inductor L2 to obtain resonance, as indicated by a maximum amplitude signal, while maintaining symmetry. See figure 80.

NOTE: It is also possible to use this procedure with machines operating on 250-cycle standards, since the tuned circuit response is broad enough to pass both the 240- and 250-cycle signals.

The alternate method of tuning inductor L2, using the audio oscillator, may also be used. The procedure is as follows:

1. Apply power to the machine (in STOP mode), and place module on module extender.

2. Attach low-capacitance oscilloscope probe to the collector of transistor Q15.

3. Inject a 240-cycle signal from the audio oscillator, through a blocking capacitor (10 μfd or greater), between the CT IN test point (TP3) and module ground.

4. Adjust 240-cycle signal amplitude at the audio oscillator to obtain a waveform of approximately 5 volts peak-to-peak, as seen on the oscilloscope.

5. Tune inductor L2 for resonance, as indicated by a maximum amplitude signal on the oscilloscope, while decreasing the input from the audio oscillator so that the waveform on the oscilloscope does not appreciably exceed 5 volts peak-to-peak.

NOTE: For machines operating on 250-cycle standards, the oscillator frequency should be 245 cps.

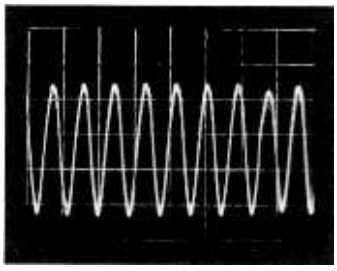


Figure 80—Inductor L2 Tuned for Maximum Amplitude Signal While Maintaining Symmetry

CAPSTAN PHASE MODULE (DOMESTIC)

Circuit Description

General

The capstan phase module (no. 320), operating only during tape playback, performs three basic servo loop functions. One of these is to divide-down the frequency of the 240-cycle pulses derived from the control track signal in the control track record/playback module (no. 319), to a pulse rate of 30 cps. This is accomplished by a chain of three binary counters, each dividing the frequency by two (see block diagram, figure 81). The 30-cycle pulses are then fed to the capstan error module (no. 321) where they are formed into sample pulses and applied to a phase comparator bridge.

A second function of the module is to reset the binary counters which divide-down the control track pulse frequency, so that the count begins in the proper phase relationship to insure alignment of tape sync with the local sync signal (station sync, etc.). This function is performed in both the switchlock and pixlock modes of servo operation. In the tonewheel mode however, the phasing of the count is random; therefore, while the machine will still "lock-up" in playback, there is only one chance in eight of beginning with the particular control track pulse which is phased so that tape and local sync signals are aligned.

The third function of the capstan phase module is to provide the circuitry required for continuous control track phase variation over a very wide range. This variation is necessary to insure that during tape playback in the tonewheel servo mode, head no. 1 can be made to play back information from the video track containing vertical sync (which is normal operating procedure), or from any of the three remaining tracks. The phase variation is obtained by adjusting the C.T. PHASE control on the PLAY control panel and, in addition to providing a means of "slipping tracks", the variable phase feature serves the important function of allowing the heads to be centered over the video track during tonewheel, switchlock, or pixlock mode of servo operation. To obtain the wide range of phase variation required, the control track pulses are applied to the binary counter chain through two cascaded delay multivibrators which in turn are controlled by constant current sources (figure 81). By adjusting the C.T. PHASE control, the effect of the constant current sources on the delay multivibrators may be varied, thus varying the phase of the control track pulses.

Control Track Phase Delay Multivibrators

Control track phase delay multivibrators Q2-Q3 and Q5-Q6 in cascade (figure 82) delay the 240-cycle control track pulse before it is used to trigger the first binary counter. The constant current source transistors Q1 and Q4 feed current into the timing circuit of each delay multivibrator, thus determining the multivibrator recovery time which in turn establishes the amount of delay inserted into the 240-cycle pulse path. The magnitude of the current fed into the multivibrator timing circuits, and therefore the amount of delay generated, is continuously variable over a range of approximately 4160 microseconds by adjusting the C.T. PHASE control. (The range of the control is such that a video head may be "slipped" plus or minus two video tracks when the control is fully rotated in either direction from its center, or zero, position.)

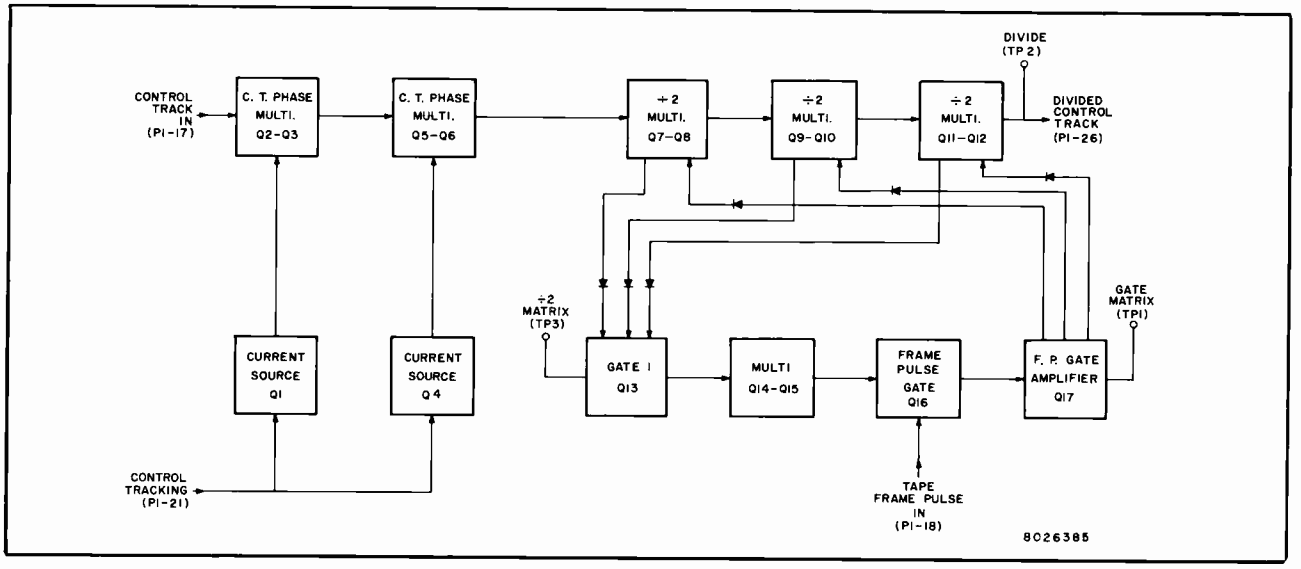
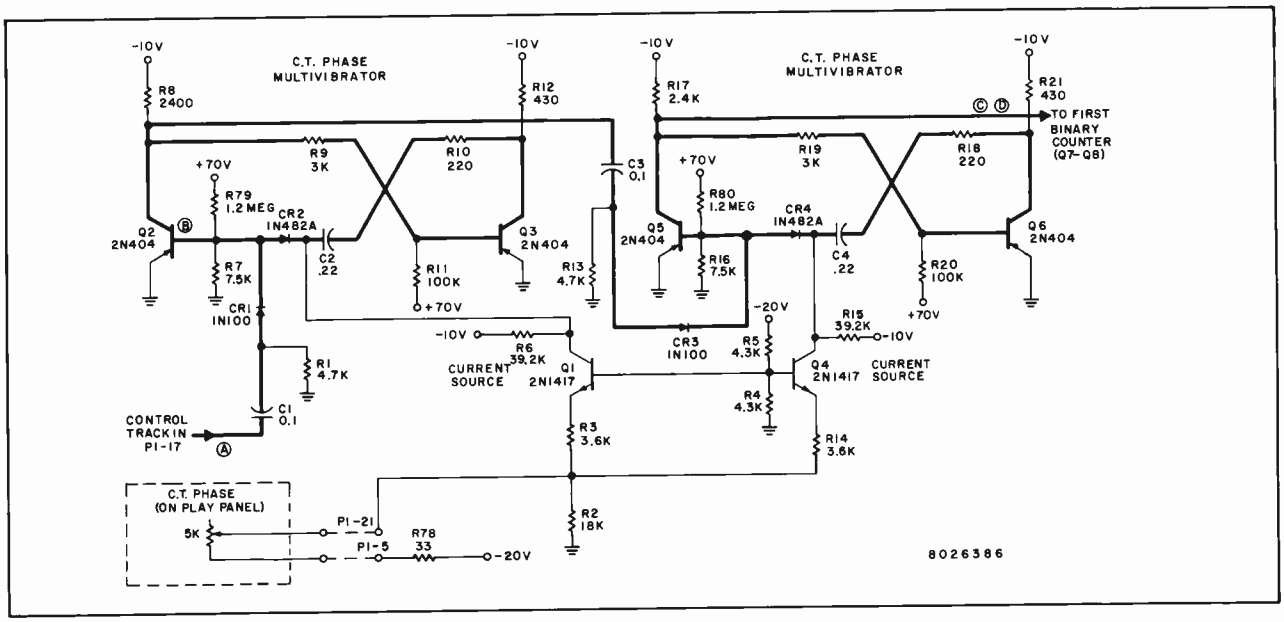
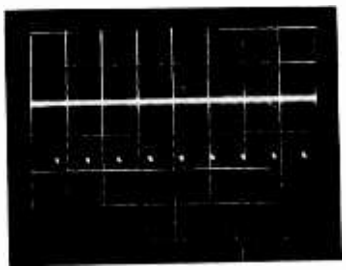
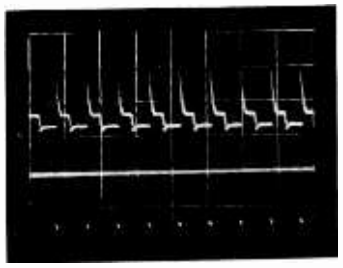


Figure 81—Capstan Phase Module Block Diagram

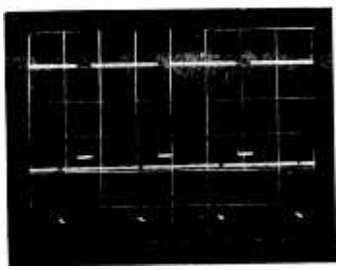




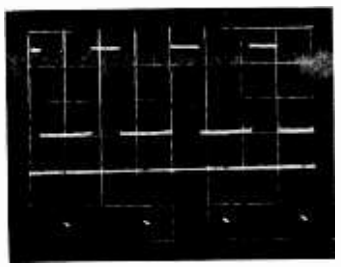
A. C.T. IN (P1-17), 5v/cm. (5 msec/cm)



B. Top: Q2 base. Bottom: C.T. IN. (5 msec/cm)



C. Top: Q5 collector (Minimum Delay). Bottom: C.T. IN.



D. Top: Q5 collector (Maximum Delay). Bottom: C.T. IN.

Machine in PLAY mode. All sweep times 2 msec/cm and amplitudes 2v/cm, unless otherwise noted.

Figure 82—Control Track Phase Delay Multivibrators

The 240-cycle negative-going control track pulses are applied to the module at pin 17 of plug P1 (figure 82A), and are differentiated by the network consisting of capacitor C1 and resistor R1 to form a series of positive- and negative-going spikes. The positive-going spikes are then fed through diode CR1 to the base of transistor Q2. Transistors Q2 and Q3 form the first of two one-shot monostable delay multivibrators which provide the delay range required for proper control track phasing. In the multivibrator normal (stable) state, diodes CR1 and CR2 are forward biased by resistor R6 returned to −10 volts. Transistor Q2 is then biased to saturation by the negative potential applied to its base from the voltage divider network consisting of resistors R6, R1 and R7 in parallel, and R79. Simultaneously, transistor Q3 is cut off by the positive potential applied to its base.

When a positive-going spike is fed to the base of transistor Q2 (figure 82B), the transistor is cut off. This causes transistor Q3 to conduct, and a positive-going pulse appears at its collector. The positive going pulse cuts off diode CR2, thereby disconnecting resistor R6 from the bias voltage network of transistor Q2. Transistor Q2 will then remain cut off, due to the small positive potential applied to its base from the divider network consisting of resistors R7 and R79. (This small positive potential also cuts off diode CR1, thus disconnecting resistor R1 from the biasing network.) As capacitor C2 charges toward −10 volts through resistor R6 (and through transistor Q1 as explained below), diode CR2, and in turn CR1, will again be forward biased. Thus the bias voltage at the base of transistor Q2 is returned to its original negative value, causing the transistor to saturate, and the multivibrator reverts to its stable state.

Normally the multivibrator recovery time (and thus the width of the output pulse at the collector of transistor Q2) would be determined by the time constant established by the values of capacitor C2 and resistor R6. However, current source transistor Q1 also acts as a charging path for capacitor C2; therefore it too affects the multivibrator recovery time and hence the output pulse width. The current supplied by transistor Q1 is determined by the bias voltage on its emitter, and this voltage may be varied between the approximate limits of −11 and −19 volts dc by adjusting the C.T. PHASE control. (The C.T. PHASE control operates as a rheostat, and is connected between the decoupled −20 volt bus and resistor R2 through pins 5 and 21 of plug P1, as shown in figure 82.) As the control is adjusted, the current fed into the multivibrator timing circuit varies; however, once the control has been set, the operation of the transistor is such that it will maintain an essentially constant current output regardless of the normal voltage variations in its collector circuit. When diode CR2 is cut off, as explained in the paragraph above, the time constant circuit is disconnected from the base circuit of transistor Q2. Thus the leakage current of transistor Q2 is prevented from influencing the timing cycle, and greater accuracy in timing is assured.

The negative pulse outputs at the collector of transistor Q2 are differentiated by the network consisting of capacitor C3 and resistor R13 to form a series of positive- and negative-going spikes. The positive-going spikes, corresponding to the delayed (positive-going) edge of the negative pulse, are fed through diode CR3 to the base of transistor Q5. Transistors Q5 and Q6 form the second control track phase multivibrator, which operates in exactly the same manner as multivibrator Q2-Q3. In this case, current source transistor Q4 supplies current to the multivibrator timing circuit and, since it is in parallel with current source transistor Q1, its current output is also controlled by the C.T. PHASE control. Thus the positive-going edge of the negative pulse output at the collector of transistor Q5 is delayed with respect to the 240-cycle control track pulse by an interval which is determined by the setting of the C.T. PHASE control. This edge is then used in triggering the first binary counter. Figure 82C shows the output at the collector of transistor Q5 with the C.T.PHASE control rotated fully counterclockwise (minimum delay), and figure 82D shows the same output with the control rotated fully clockwise (maximum delay).

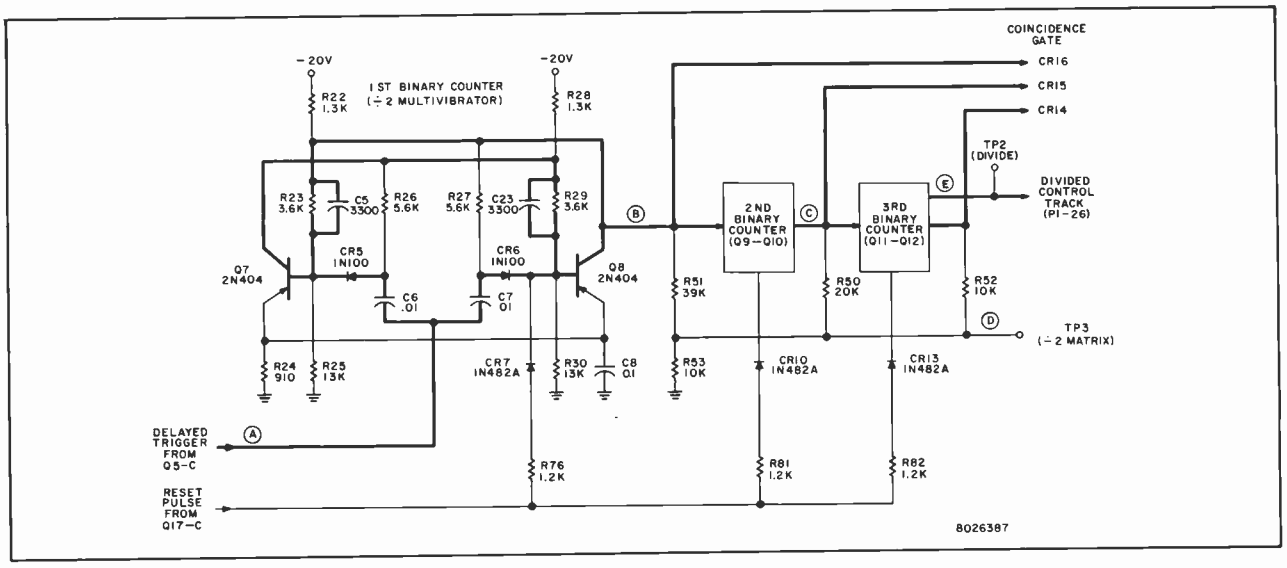
Binary Counters

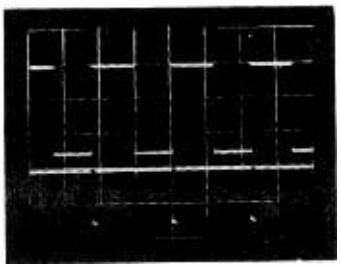
Three identical binary counter circuits in cascade divide-down the delayed 240-cycle control track pulse to a 30-cycle output (figure 83). The binary counter circuits are conventional bistable multivibrators; i.e., each half of the multivibrator is driven by the same input signal. In the particular type of binary counter circuit used in this module, a positive-going pulse edge cuts off the conducting transistor which in turn drives the non-conducting transistor to saturation. The transistors will remain in this state until the next positive-going pulse edge appears and reverses the condition. The output at the collector of either transistor will then be alternately positive- and negative-going; thus the desired divide-by-two action is achieved.

The negative pulse at the collector of transistor Q5 (figure 83A) is fed through capacitors C6 and C7, and the positive-going edge triggers the first binary counter (Q7-Q8). The output at the collector of transistor Q8 (figure 83B) drives the second binary counter (Q9-Q10) and, finally, the output at the collector of transistor Q10 (figure 83C) drives the third binary counter (Q11-Q12).

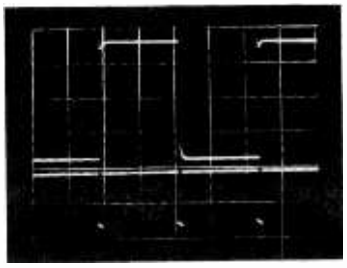
The outputs at the collectors of transistors Q8, Q10, and Q12 are fed to the diode gating circuit consisting of diodes CR16, CR15, and CR14, which produces an output only when all three collector potentials are at their most negative level. Resistors R50, R51, R52, and R53 form a matrix network in which the three output signals (from Q8, Q10, and Q12) are combined into a stairstep waveform, as shown in figure 83D, when all counters are operating properly. This waveform may be observed at test point TP3 (÷2 MATRIX).

The square wave signal at the collector of transistor Q12 (in the third binary counter) having a level which varies between the approximate limits of −8 and −13 volts, represents division of the 240-cycle

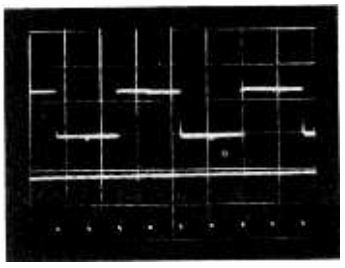




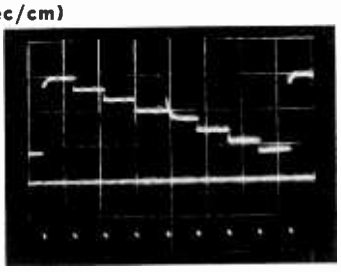
A. Top: Q5 collector (Normal Delay). Bottom: C.T. IN (P1-17). (2 msec/cm)



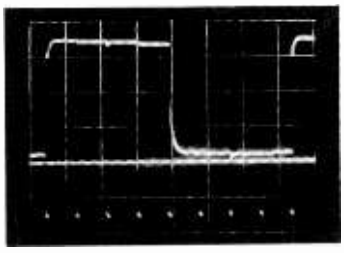
B. Top: Q8 collector. Bottom: C.T. IN. (2 msec/cm)



C. Top: Q10 collector, 5v/cm. Bottom: C.T. IN.



D. Top: TP3 (÷2 MATRIX). Bottom: C.T. IN.



E. Top: Q12 collector. Bottom: C.T. IN.

Machine in PLAY mode. All sweep times 5 msec/cm and amplitudes 2v/cm, unless otherwise noted.

Figure 83—Binary Counters

control track pulses by eight and may be observed at test point TP2 (DIVIDE). This signal (figure 83E) appears at pin 26 of plug P1 and is fed to the capstan error module (no. 321) where a sample pulse is formed from the positive-going edge of the square wave when the machine is operated in the PLAY mode. (The sample pulse thus formed is applied to a phase comparator circuit in the capstan error module, which derives the error signal used in controlling the capstan motor speed.)

The counters may be reset by applying a positive-going pulse through diodes CR7, CR10, and CR13 to transistors Q8, Q10, and Q12 respectively. If any of these transistors are conducting when the positive-going reset pulse is applied, the pulse will cut it off; if none are conducting, the pulse will have no effect. Therefore, the application of a positive-going pulse to each of the transistors simultaneously will insure that the second transistor of each binary counter is cut off, thus causing the count to begin from a known state when the next delayed control track pulse is applied to the base of transistor Q8.

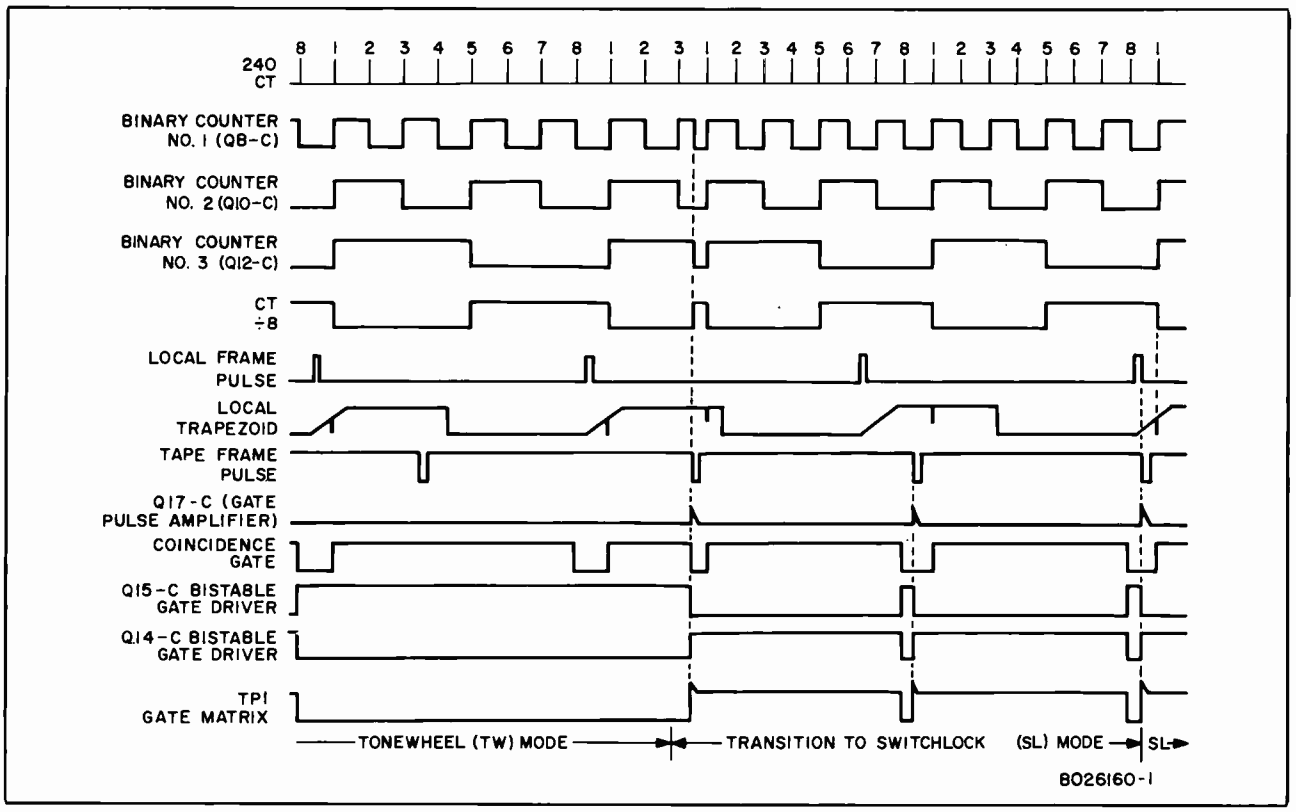


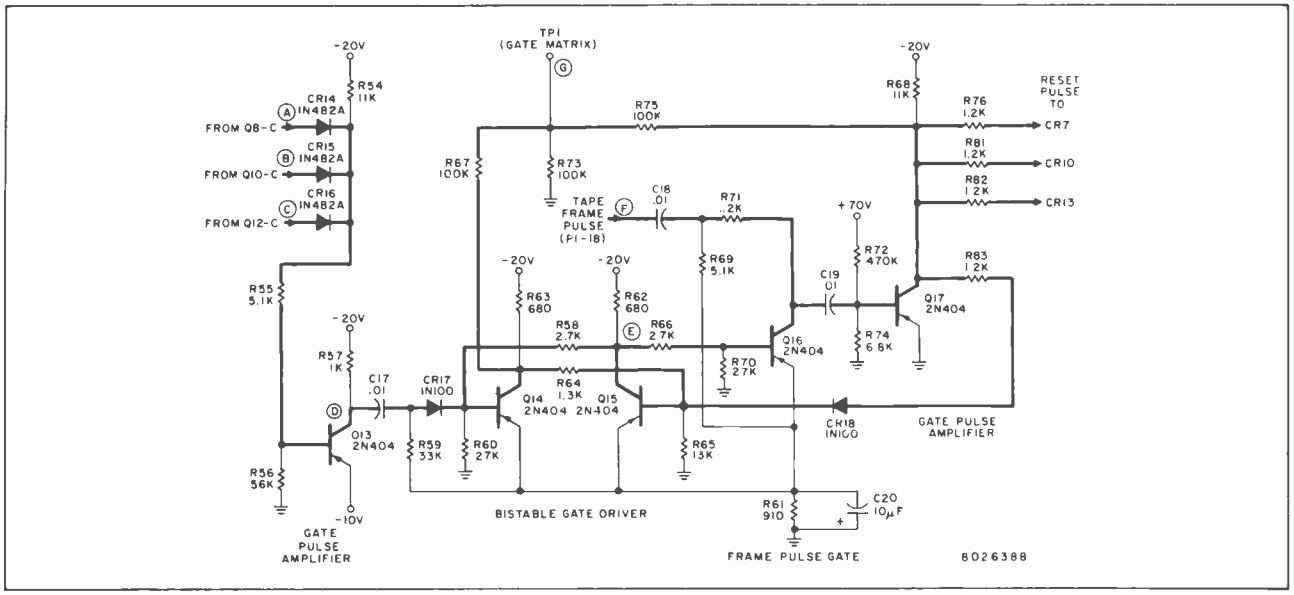
Figure 84—Timing Diagram Indicating Gating Action During Transition from Tonewheel to Switchlock Mode

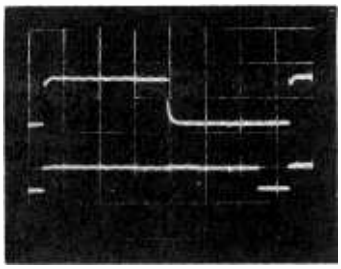
Reset Pulse Gating Circuits

Reference to the timing diagram, figure 84, will clarify the following description of the reset pulse formation and the action of the gating circuits in locking the tape vertical sync to local vertical sync. Approximately the first one-third of the diagram shows the timing obtained during normal tonewheel servo operation with the capstan motor running at normal speed. When the machine is operated in switchlock (or pixlock) servo mode, the capstan motor is forced to speed up (in the example shown) until switchlock is achieved, as shown at the extreme right. To conserve space on the diagram, the transition from tonewheel to switchlock modes is shown as covering two cycles; however, many more cycles are actually required because the inertia of the capstan motor prevents it from changing speed rapidly.

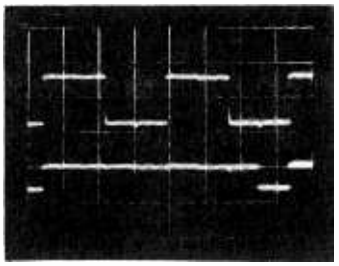
The input control track pulses and the outputs from each of the three binary counters are shown at the top of the timing diagram. The ÷8 waveform, appearing at the collector of transistor Q12 in the third binary counter, is used in generating a sample pulse (in the capstan error module) which is timed such that it appears at the center of the local reference trapezoid slope. (The local reference trapezoid is generated in the capstan error module from the reference frame pulse.) A tape frame pulse is shown on the timing diagram in one of the eight possible positions it may assume when the machine is operated in the tonewheel servo mode. Waveforms below the tape frame pulse in this section of the diagram are not significant during tonewheel servo operation because the tape frame pulse is applied to the capstan phase module only when operating in switchlock (or pixlock) servo mode.

As shown in figure 85, the outputs at the collectors of transistors Q8, Q10, and Q12 in the binary counter circuits are fed to diodes CR16, CR15, and CR14 of the coincidence gate (figures 85A, B, C). The voltage swing on each of the collectors varies from −8 to −15 volts. When the voltage on any of the three collectors reaches −8 volts, the diode connected to that particular collector will conduct, thereby clamping the voltage at the common cathode connection of the diodes at −8 volts. This voltage is then applied to the base of gate pulse amplifier transistor Q13 and cuts the transistor off. The transistor will remain cut off as long as the negative potential is applied to its base. However, when all three collector voltages are at −15 volts simultaneously (coincidence) the diodes will be reverse-biased; the voltage at the common cathode connection of the diodes will fall to approximately

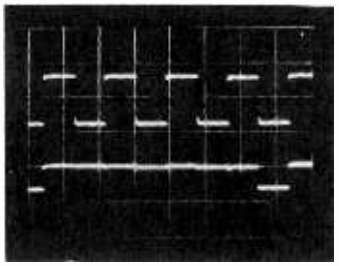




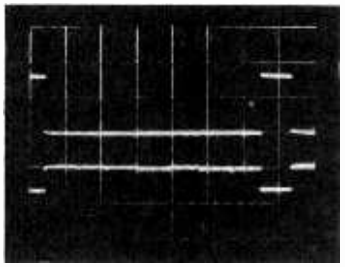
A. Top: CR14 anode.
Bottom: CR14 cathode.



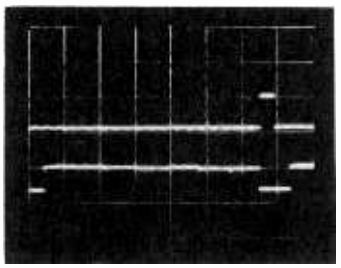
B. Top: CR15 anode.
Bottom: CR14 cathode.



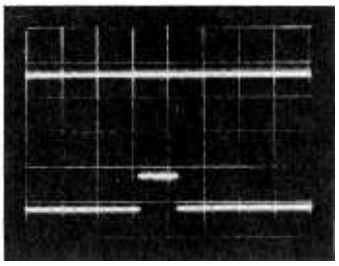
C. Top: CR16 anode.
Bottom: CR14 cathode.



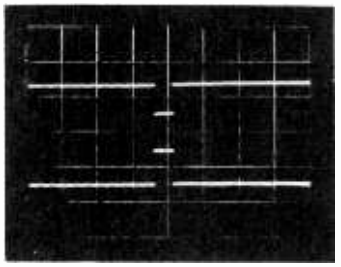
D. Top: Q13 collector.
Bottom: CR14 cathode.



E. Top: Q15 collector.
Bottom: CR14 cathode.



F. Top: Tape Frame Pulse (P1-18), 10v/cm.
Bottom: Q15 collector.
(2 msec/cm)



G. Top: TP1 (GATE MATRIX), 2v/cm.
Bottom: Q15 collector (Coincidence).
(2 msec/cm)

Machine in PLAY/SL mode. All sweep times 5 msec/cm and amplitudes 5v/cm, unless otherwise noted.

Figure 85—Reset Pulse Gating Circuits

−13 volts, as determined by resistors R54 and R55; and transistor Q13 will conduct. The voltage at the collector of transistor Q13 rises from −20 volts when the transistor is cut off to −10 volts when it is conducting (figure 85D).

The coincidence pulse formed by the voltage variation at the collector of transistor Q13 is differentiated, and the positive-going spike generated from its leading edge is fed through diode CR17 to the base of transistor Q14. Transistors Q14 and Q15 form the bistable gate driver, which is a bistable multivibrator operating in a manner similar to the binary counters except that each transistor is driven from a separate source. If transistor Q14 is conducting (transistor Q15 cut off), a positive-going pulse from the coincidence gate amplifier (transistor Q13) will reverse this condition by cutting off Q14, which in turn causes Q15 to conduct (figure 85E). Subsequent positive-going coincidence pulses will have no effect on the multivibrator; therefore transistors Q14 and Q15 will remain in the above state indefinitely.

While transistor Q15 is conducting, its collector is at the same potential as its emitter. Consequently, the voltage fed through the voltage divider network consisting of resistors R66 and R70 to the base of frame pulse gate transistor Q16 will be positive with respect to its emitter voltage since the emitter of Q16 is at the same potential as the emitter of transistor Q15. Transistor Q16 will then be held in the cut-off state, thereby allowing the tape frame pulse (generated in the tape sync processor module, no. 317) to be applied to the base of frame pulse gate amplifier transistor Q17 when the machine is operated in switchlock (or pixlock) servo mode (figure 85F). When the machine is operated in the tonewheel servo mode, the tape frame pulse is not applied to the capstan phase module and no further action takes place.

Transistor Q17, which is biased at cut-off, will be driven to saturation when the negative-going tape frame pulse is applied to its base from pin 18 of plug P1. This generates a positive-going pulse at the collector of Q17 which is fed simultaneously to the three reset diodes (CR7, CR10, and CR13) of the binary counter circuits and to the base of transistor Q15 through diode CR18. The positive-going pulse fed to the base of transistor Q15 cuts the transistor off, and this in turn simultaneously drives transistors Q14 and Q16 into conduction. When transistor Q16 conducts, it provides a short circuit for the frame pulse almost immediately after the frame pulse appears, thereby permitting transistor Q17 to return to the cut-off state. Since only a very small portion of the frame pulse appears at the base of transistor Q17, the output (reset pulse) at its collector is consequently very narrow (roughly one or two microseconds wide). The actual width of the reset pulse is determined by the delay in the loop (from transistor Q17 to Q15 to Q16).

When the reset pulse is applied to each binary counter, the counters will be placed in the proper state to begin a new count with the next succeeding control track pulse. This action then generates a positive-going coincidence pulse which is applied to the base of transistor Q14 almost simultaneously with the application of a reset pulse to the base of transistor Q15. However, the effect of the reset pulse in cutting off transistor Q15 (which drives transistor Q14 to saturation) overrides the effect of the coincidence pulse attempting to cut off Q14. Therefore, the bistable gate driver transistors Q14 and Q15 will remain in a stable state with Q14 conducting and Q15 cut off until the next coincidence occurs and generates a pulse to reverse this state. During this entire time, transistor Q16 is biased so that it will conduct and thereby short out any noise pulses which may occur between the desired tape frame pulses. This will prevent noise from inadvertently triggering transistor Q17 and upsetting the binary counters. Each succeeding tape frame pulse will occur during coincidence, so that the reset pulse does not disturb the binary counters which have been started on the proper count.

The ÷8 output, fed to the capstan error module from pin 26 of plug P1, will generate a sample pulse at the beginning of a new count. (This is shown on the timing diagram, figure 84, as occurring during the positive maximum of the local reference trapezoid.) The resultant error signal causes the capstan motor to speed up (in the example shown). The increase in tape speed in turn causes the frequency of the control track pulses to increase, thereby moving them closer together with respect to the fixed reference trapezoid waveform. The tape frame pulse, which bears a fixed relationship to the control track pulses, also increases in frequency. Therefore, at the beginning of the next count, the sample pulse will occur closer to the trapezoid slope. After a number of such cycles (not shown on the diagram), the sample pulse will fall on the trapezoid slope, and the capstan motor will "lock-in" at its normal speed. The last column of pulses on the diagram (at the extreme right) shows the pulse relationships at the beginning of a switchlock cycle.

Test point TP1 (GATE MATRIX) is provided as a convenient point for checking the operation of the reset pulse and bistable gate driver circuits. At test point TP1 the outputs of these circuits are added together and the waveform should appear as shown in figure 85G when the machine is operated in the switchlock (or pixlock) servo mode.

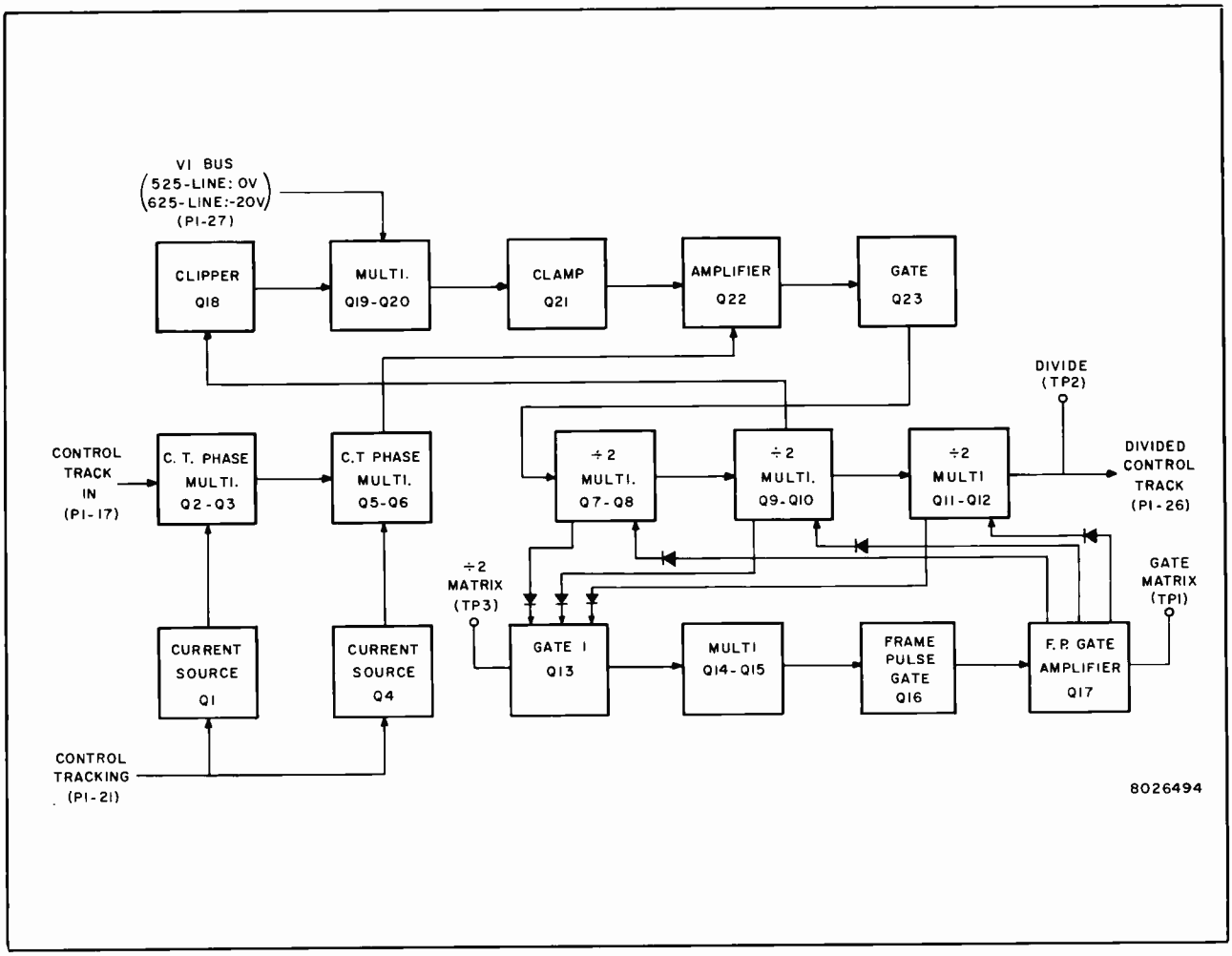


Figure 86—Capstan Phase Module (International) Block Diagram

CAPSTAN PHASE MODULE (INTERNATIONAL)

Circuit Description

General

The International version of the capstan phase module (no. 320) differs from the domestic version in that additional circuitry has been added to the module to accommodate 405/625/819-line (International) standards as well as the conventional 525-line standards. The difference in modules consists mainly of the fifth-pulse eliminator circuitry which has been added to the International module (figure 86) and is utilized only when the machine is operated on one of the International (50-cycle) standards. It is the function of the fifth-pulse eliminator circuitry to suppress every fifth pulse in each series of ten input control track pulses fed to the module, so that only eight of the ten pulses reach the binary counters. The binary counters then operate as they do on 525-line standards, providing one negative-going output pulse for every eight trigger pulses which are derived from the ten input control track pulses (figure 87). Thus the 250-cycle input control track pulses are divided-down to a 25-cycle rate.

Whether the module operates on 525-line or International standards is determined by the switch on the International vertical advance module (no. 228). In the 525-line position, the VI bus is at ground potential. This prevents the fifth-pulse eliminator circuitry from operating and the module then functions exactly as does the domestic version. When the switch is in the 405- or 625-line position, for example, the VI bus is at −20 volts dc and the fifth-pulse eliminator circuits function as described below.

The *control track phase delay multivibrators, binary counters,* and *reset pulse gating circuits* operate identically on either 525-line or International standards. For the description of these circuits, refer to the

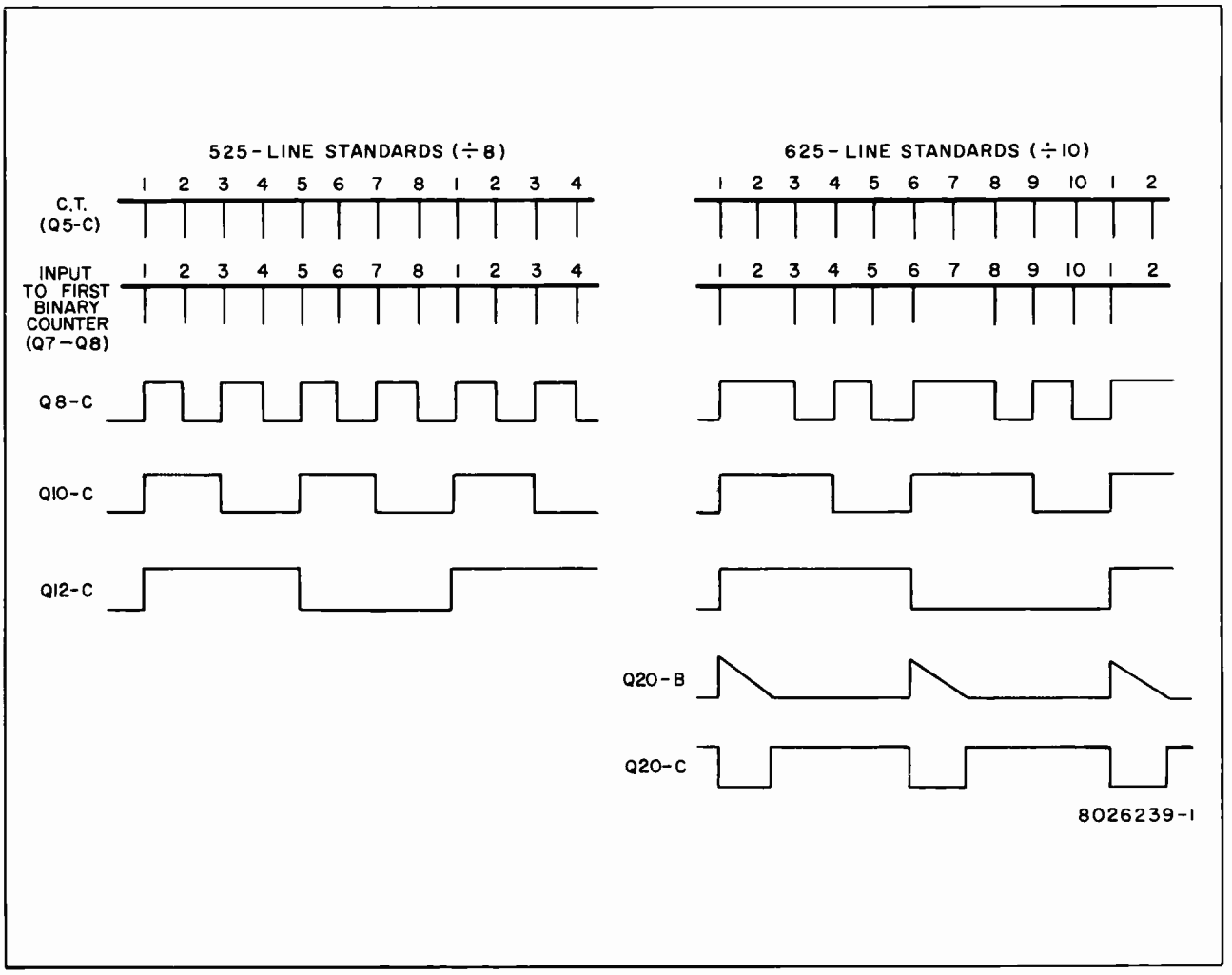


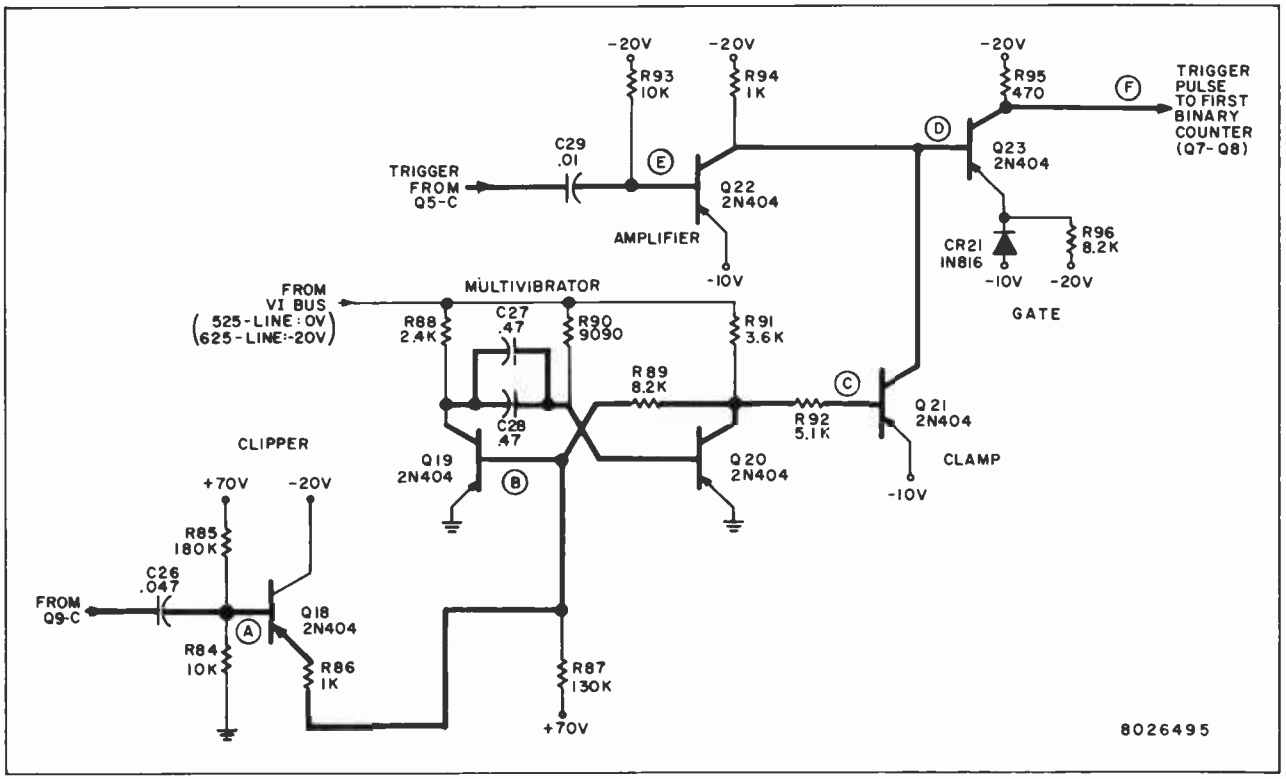
Figure 87—Timing Diagram Comparing Counter Operation on 525- and 625-Line Standards

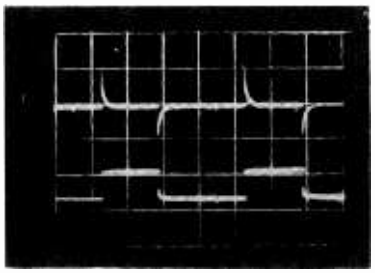
capstan phase, domestic, module discussion. Note that during operation on International standards, the appropriate timing differences must be taken into consideration; e.g., the 240-cycle control track pulse rate becomes a 250-cycle rate, etc.

Fifth-Pulse Eliminator

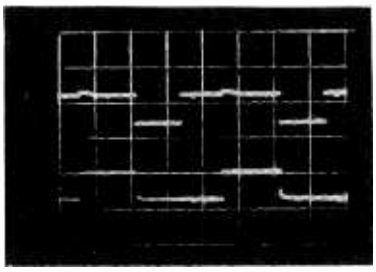
The fifth-pulse eliminator circuit (figure 88) suppresses every fifth control track pulse when the machine is operating on International standards, so that the same cascaded binary counters used during operation on 525-line standards may then be used in obtaining a division by ten. The operation of the circuit depends upon the potential applied to the module through pin 27 of plug P1 from the VI bus, and this potential in turn is controlled by the line standards switch on the International vertical advance module (no. 228).

Transistors Q19 and Q20 form a one-shot monostable multivibrator. In the multivibrator stable state, transistor Q19 is cut off and requires a negative-going pulse from emitter follower transistor Q18 to trigger it into conduction and thus begin the multivibrator action. When the machine is operated on 525-line standards, the VI bus (and therefore the junction of resistors R88, R90, and R91) is at ground potential. The supply voltage is thereby removed, and the multivibrator is prevented from functioning. This action places the bias voltage on the base of transistor Q21 at approximately ground potential (actually slightly positive) and the transistor is held in cut-off by the negative potential on its emitter. Thus the delayed control track pulses from the collector of transistor Q5 are allowed to pass unimpeded through transistors Q22 and Q23 before returning to trigger the first binary counter (Q7-Q8).

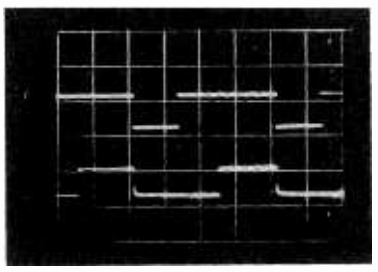




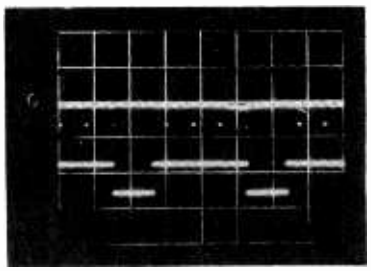
A. Top: Q18 base.
Bottom: Q9 collector.



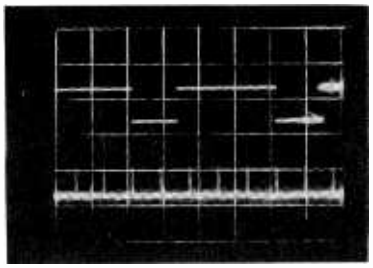
B. Top: Q19 base, 5v/cm.
Bottom: Q9 collector.



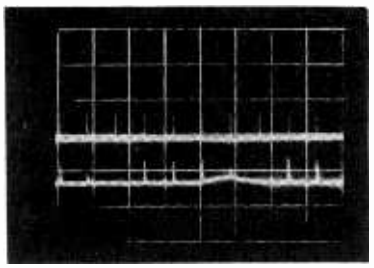
C. Top: Q21 base.
Bottom: Q9 collector.



D. Top: Q23 base, 2v/cm.
Bottom: Q21 base.



E. Top: Q21 base.
Bottom: Q22 base, 5v/cm.



F. Top: Q22 base, 5v/cm.
Bottom: Q23 collector, 1v/cm.

Machine in PLAY/SL mode. All sweep times 5 msec/cm, and amplitudes 10v/cm, unless otherwise noted.

Figure 88—Fifth Pulse Eliminator

When the machine is operated on International standards, the VI bus is at −20 volts dc and the one-shot multivibrator Q19-Q20 is operative. The bias voltage on transistor Q19 is still positive, and Q19 is thus held in cut-off. However, a negative-going pulse from emitter follower transistor Q18 will now drive transistor Q19 into conduction, thus initiating multivibrator action so that the fifth-pulse eliminator circuit is allowed to function.

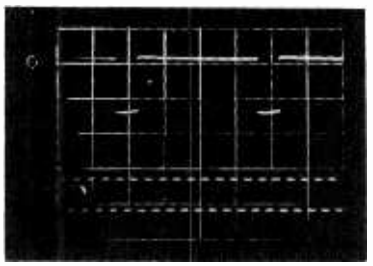
At the beginning of each new count, during International operation, the negative-going pulse at the collector of transistor Q9 in the second binary counter circuit is differentiated by the network consisting of capacitor C26 and resistor R84. The resulting positive- and negative-going spikes are then fed to the base of clipper transistor Q18 (figure 88A) whose purpose is to isolate multivibrator Q19-Q20 from the binary counter circuit. Transistor Q18 is normally biased at cut-off by the positive potential applied to its base from the voltage divider network consisting of resistors R84 and R85. When a negative-going spike appears at its base, the transistor is driven into conduction and a negative-going pulse appears at its emitter. This pulse is fed to the base of transistor Q19, in the multivibrator circuit, and drives the transistor into conduction (figure 88B).

When transistor Q19 is driven into conduction, transistor Q20 is simultaneously cut off and will remain off for a length of time determined by the charging of capacitors C27 and C28 in parallel through resistor R90. The value of this RC time constant is such that transistor Q20 will remain cut off for approximately 6 milliseconds, an interval which is roughly 1½ times the period of the control track pulses. The negative pulse developed at the collector of transistor Q20 when the transistor is cut off is fed to the base of clamping transistor Q21 (figure 88C). This pulse causes Q21 to conduct, thereby shorting out the signal at the base of gating transistor Q23. Therefore, the second control track pulse (which occurs during the multivibrator timed period) is shorted out and does not appear at the base of Q23 (figure 88D). At the end of the timed period multivibrator Q19-Q20 reverts to its stable state, again cutting off clamping transistor Q21 which in turn allows the control track pulses to pass. Since this action is initiated in the second binary counter, it will be repeated on the 6th control track pulse, thus the 7th pulse will also be shorted out.

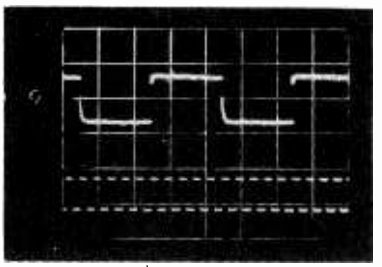
The output at the collector of gating transistor Q23 will therefore be a train of pulses from which the 2nd and 7th pulses have been eliminated (figure 88F). Since the binary counter chain requires eight input pulses before it will deliver an output, and two pulses in every eight are eliminated by the clamping action of transistor Q21, a total of ten input pulses will now be required for each output, and thus the desired ÷10 action is obtained. The binary counters will function as they do on 525-line standards except that the periods initiated by the 1st and 6th pulses will be twice as long when operating on International standards.

Note that the 1st and 6th pulses appearing at the collector of transistor Q23 are much narrower than the remaining pulses. This is because clamping transistor Q21 shorts out the remainder of the pulse soon after the pulse leading edge has triggered the binary counters, which in turn trigger the monostable multivibrator Q19-Q20.

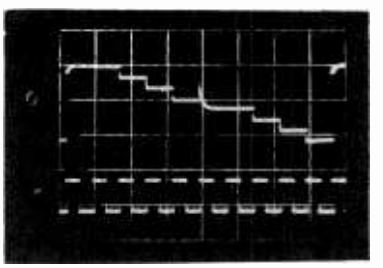
Waveforms appearing at test points TP1 (GATE MATRIX), TP2 (DIVIDE), and TP3 (÷2 MATRIX) are shown in figure 89A, B, and C. These waveforms have been obtained while operating the machine on 625-line standards in the switchlock servo mode.



A. Top: TP1 (GATE MATRIX), 1v/cm. Bottom: Q5 collector. (5 msec/cm)



B. Top: TP2 (DIVIDE). Bottom: Q5 collector. (5 msec/cm)



C. Top: TP3 (÷2 MATRIX), 2v/cm. Bottom: Q5 collector. (5 msec/cm)

Figure 89—Waveforms Obtained at Capstan Phase Module (International) Test Points on 625-Line Standards

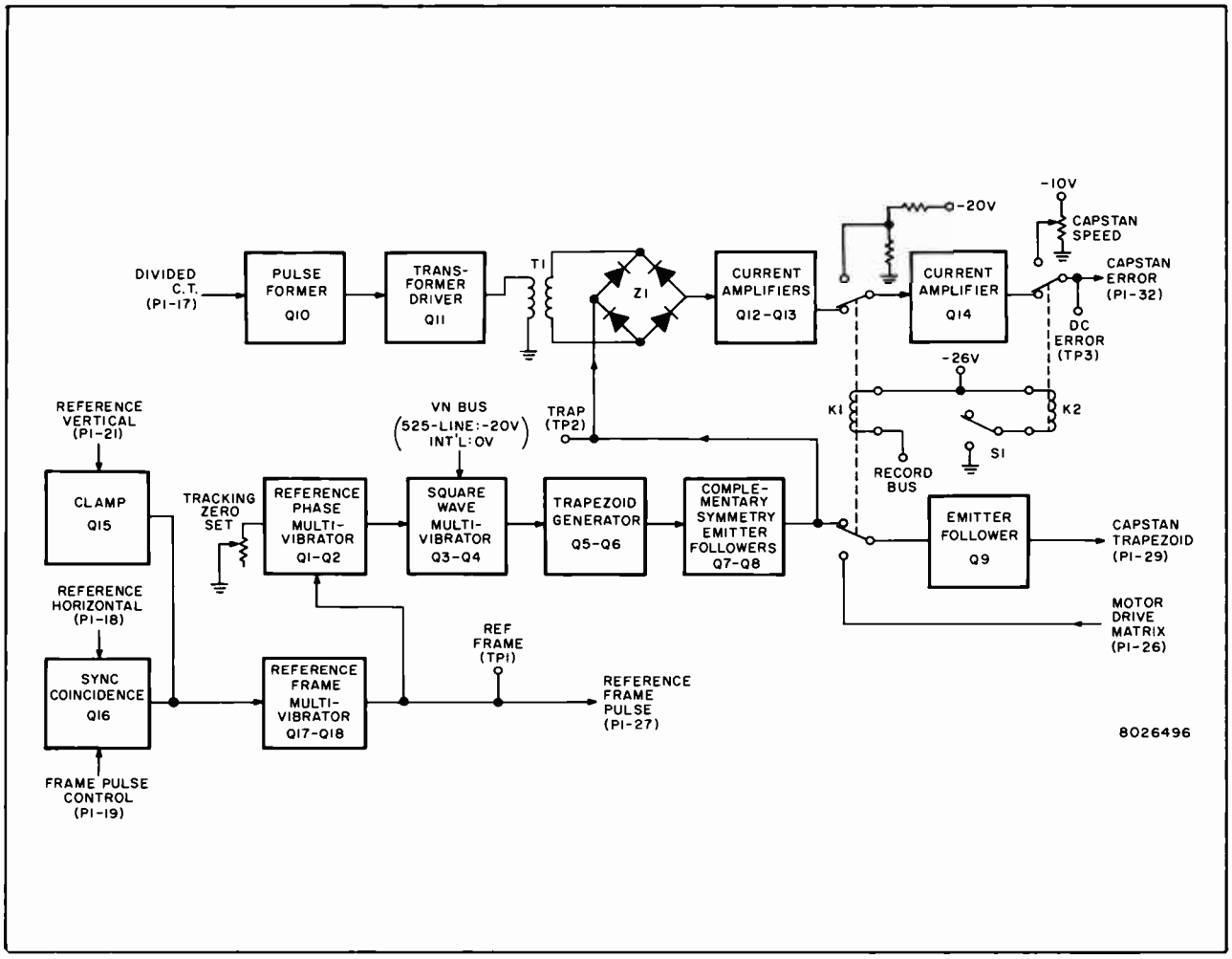


Figure 90—Capstan Error Module Block Diagram

CAPSTAN ERROR MODULE

Circuit Description

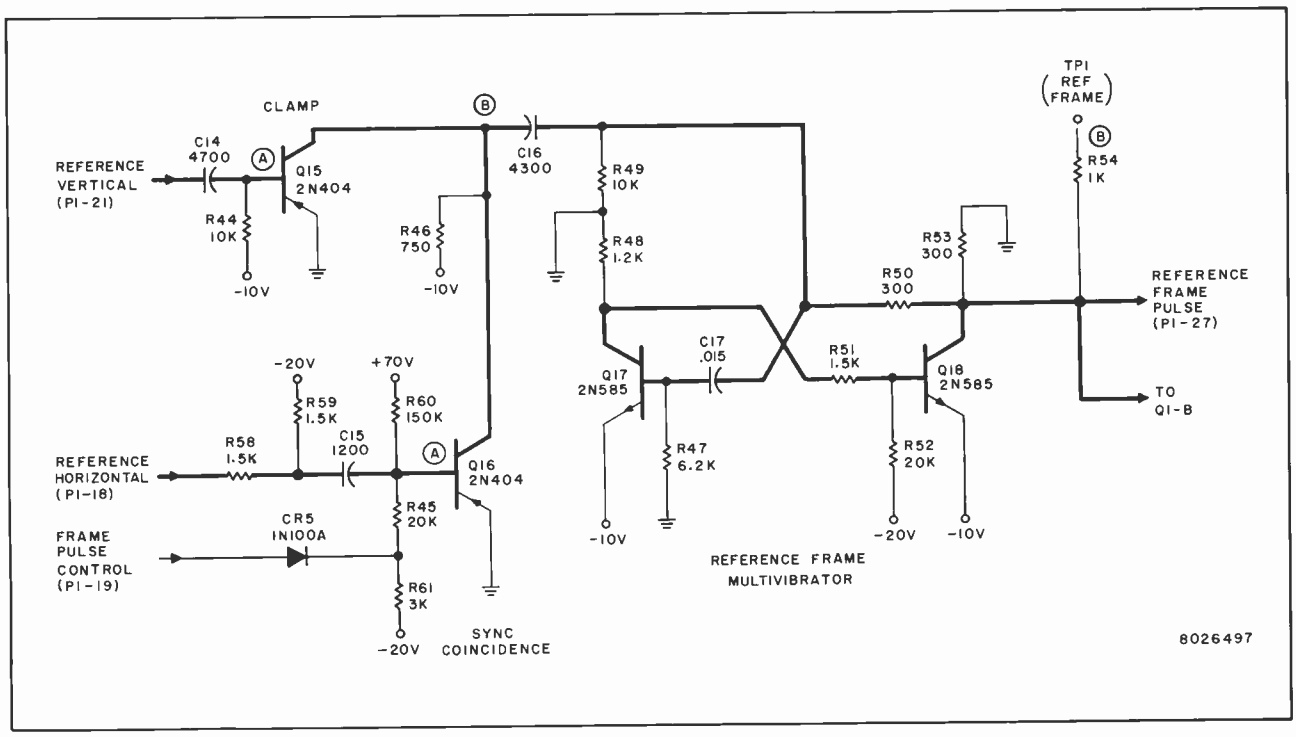
General

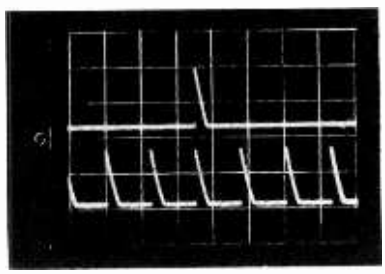
The primary function of the capstan error module (no. 321) is to generate a local stable timing reference pulse, during tape playback, which is then compared in a phase comparator bridge with the divided-down control track pulse from the capstan phase module (no. 320) to form the capstan error signal. (Refer to the block diagram, figure 90.) This signal is fed to the capstan oscillator module (no. 322), where it is used in controlling the oscillator frequency which in turn determines the capstan motor speed.

The servo reference pulse is generated from a comparison of local reference horizontal and reference vertical pulses in a coincidence gate circuit. If local sync is not available for comparison purposes, the power line frequency may be utilized in generating a servo reference. In the RECORD mode, the generated reference pulse is fed directly to the control track REC/PB module (no. 319) where it is combined with the control track signal before being recorded on the tape.

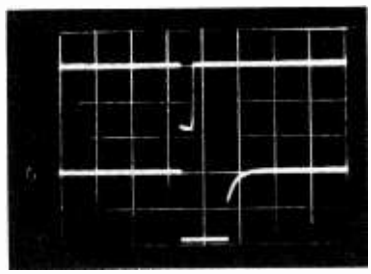
> NOTE: When the machine is playing back tape using an external servo reference, the reference pulse occurs at a frame rate (e.g., 30 cps). However, when the machine is playing back tape using line servo reference, the reference pulse occurs at a field rate (e.g., 60 cps). To avoid confusion, the servo reference pulse will be referred to as the *frame* pulse throughout the following circuit description except where specific mention is made of machine operation using *line* servo reference.

In addition to the circuits mentioned above, the capstan error module includes a circuit which is used to drive the CRO monitor so that it is possible to observe the capstan trapezoid and sample pulse waveform (in PLAY mode) or the capstan motor drive





A. Top: Q15 base, 2v/cm. Bottom: Q16 base.



B. Top: Q15-Q16 collector (Coincidence). Bottom: Q18 collector (Reference Frame Pulse).

Machine in PLAY mode. All sweep times 50 μsec/cm and amplitudes 5v/cm, unless otherwise noted.

Figure 91—Reference Frame Pulse Generator

sine wave (in the RECORD mode) on the CRO monitor when the CAP SERVO pushbutton on the CRO monitor switcher is depressed.

The push-to-operate CAPSTAN SPEED control, located on the module front panel, is provided as a means of manually controlling the capstan motor speed during tape playback. The purpose of this control is to synchronize two tape machines which are playing back identical tapes simultaneously. (If one of the machines is "on the air", the CAPSTAN SPEED control on the second or back-up machine may be used to obtain "lip synchronization" by manually varying the tape speed until the two machines are synchronized.)

Reference Frame Pulse Generator

When the machine is operated in the PLAY mode with external servo reference (e.g., sync provided by the local station sync generator), the reference frame pulse generator circuit (figure 91) combines reference vertical and reference horizontal signals in a coincidence gate circuit, and produces a stable reference timing pulse (frame pulse). The positive-going reference vertical pulse (derived from local vertical sync in the reference generator module, no. 312) is fed to the capstan error module through pin 21 of plug P1. Capacitor C14 and resistor R44 differentiate the incoming pulse before it is fed to the base of clamping transistor Q15. Transistor Q15, normally saturated,

is driven into cut-off by the positive-going spike (corresponding to the trailing edge of the incoming reference vertical pulse) fed to its base (figure 91A). This action would normally produce a negative-going pulse at the collector of Q15; however, since sync coincidence transistor Q16 is also normally saturated (as described below) and transistors Q15 and Q16 have a common collector circuit, there will be an output signal only when both transistors are cut off simultaneously (coincidence).

The negative-going reference horizontal pulse (derived from local horizontal sync in the reference generator module) occurs at a line frequency rate and is fed to the capstan error module at pin 18 of plug P1. Capacitor C15 and resistors R45 and R61 form a network which differentiates the incoming horizontal pulse before it is fed to the base of sync coincidence transistor Q16 (figure 91A, bottom). Transistor Q16 is normally saturated due to the negative bias voltage applied to its base from the voltage divider network consisting of resistors R60, R45, and R61. The positive-going spike (corresponding to the leading edge of the differentiated incoming pulse) drives Q16 into cut-off and would normally result in a negative-going pulse output at the collector of Q16. However, as mentioned in the above paragraph, transistors Q15 and Q16 must both be cut off simultaneously (coincidence) to produce an output pulse. Because of the interlacing effect, the phase relationships between the input horizontal and vertical reference pulses are such that coincidence will occur only during every other TV field (i.e., at a frame rate). Therefore, the output at the common collectors of transistors Q15 and Q16 will be a very narrow, negative-going 30-cycle pulse (figure 91B). (In International machines operating with a 50-cycle field rate, the frame pulse occurs at a 25-cycle rate.)

When external servo reference is used, as in the above description, the frame pulse control voltage is −26 volts dc. This voltage is fed, via the reference generator module, through pin 19 of plug P1 to the anode of diode CR5 and cuts the diode off. Therefore, diode CR5 has no effect on the circuit during tape playback with external servo reference. However, when line servo reference is used, pin 19 is at ground potential and diode CR5 is thus forward biased. In this case, transistor Q16 is biased at cut-off by the positive potential applied to its base from the voltage divider network consisting of resistors R60 and R45. Since there is no reference horizontal signal when line servo reference is used, transistor Q16 will remain cut off and will have no effect on the circuit. The reference vertical input is a 60-cycle pulse (developed in the reference generator module) which is differentiated by capacitor C14 and resistor R44. The positive-going spike, resulting from the differentiation, drives normally saturated transistor Q15 into cut-off. Since transistor Q16 is held in cut-off by diode CR5, a negative-going, 60-cycle pulse will appear in the common collector circuit of transistors Q15 and Q16. (In International machines operating with a 50-cycle field rate, the output pulse occurs at a 50-cycle rate.)

> NOTE: Machines supplied with 50-cycle power can only use the line frequency as a servo reference when operating on one of the International standards. In addition, machines supplied with 60-cycle power can only use the line frequency as a servo reference when operating on 525-line standards.

The negative-going output pulse, occurring at a 30- or 60-cycle rate (depending upon the servo reference used), is applied to the monostable reference frame pulse multivibrator Q17-Q18 as a triggering pulse. (On International standards the triggering pulse occurs at a 25- or 50-cycle rate.) In the multivibrator stable state, transistor Q17 is saturated by the negative potential at its emitter with respect to that at its base, and transistor Q18 is cut off by the negative potential applied to its base from the voltage divider network consisting of resistors R52, R51, and R48. When the negative-going pulse output from the coincidence circuit is fed to the base of transistor Q17 it cuts the transistor off, thus beginning the multivibrator action. The "off" time of the multivibrator is determined by the time constant developed as capacitor C17 discharges through resistor R47. The output at the collector of transistor Q18 is thus a negative-going frame pulse having a width of 60 ±10 microseconds. (When using line servo reference, the output at the collector of Q18 is a field pulse having the same width as the frame pulse.) The frame pulse may be observed at test point TP1 (REF FRAME) and is shown in figure 91B (bottom).

From the collector of transistor Q18, the frame pulse is fed to the control track REC/PB module (no. 319), and to the reference phase multivibrator in the reference trapezoid generator circuit (see below). The frame pulse is combined with the control track signal in the control track REC/PB module (no. 319), and the combined signal is recorded on the tape when the machine is operated in the RECORD mode. The frame pulse thus recorded conforms to SMPTE specifications with regard to width and phasing, and may therefore be utilized for tape editing purposes.

Reference Trapezoid Generator

The reference trapezoid generator circuits (figure 92) utilize the reference frame pulse in developing a reference trapezoid waveform. The trapezoid waveform is then applied to a phase comparator bridge circuit which produces the error signal used in the capstan oscillator module to control the capstan motor speed. Reference to the timing diagram (figure 93) will clarify the following description of the trapezoid generating circuits.

The negative-going reference frame pulse from the reference frame multivibrator is a-c coupled to the reference phase multivibrator circuit by capacitor C1 and resistor R1. The negative-going, or leading edge, of the frame pulse is passed through diode CR1 to the base of transistor Q1. Transistors Q1 and Q2 combine to form the monostable reference phase multivibrator, whose purpose is to insert an adjustable delay into the reference frame pulse path.

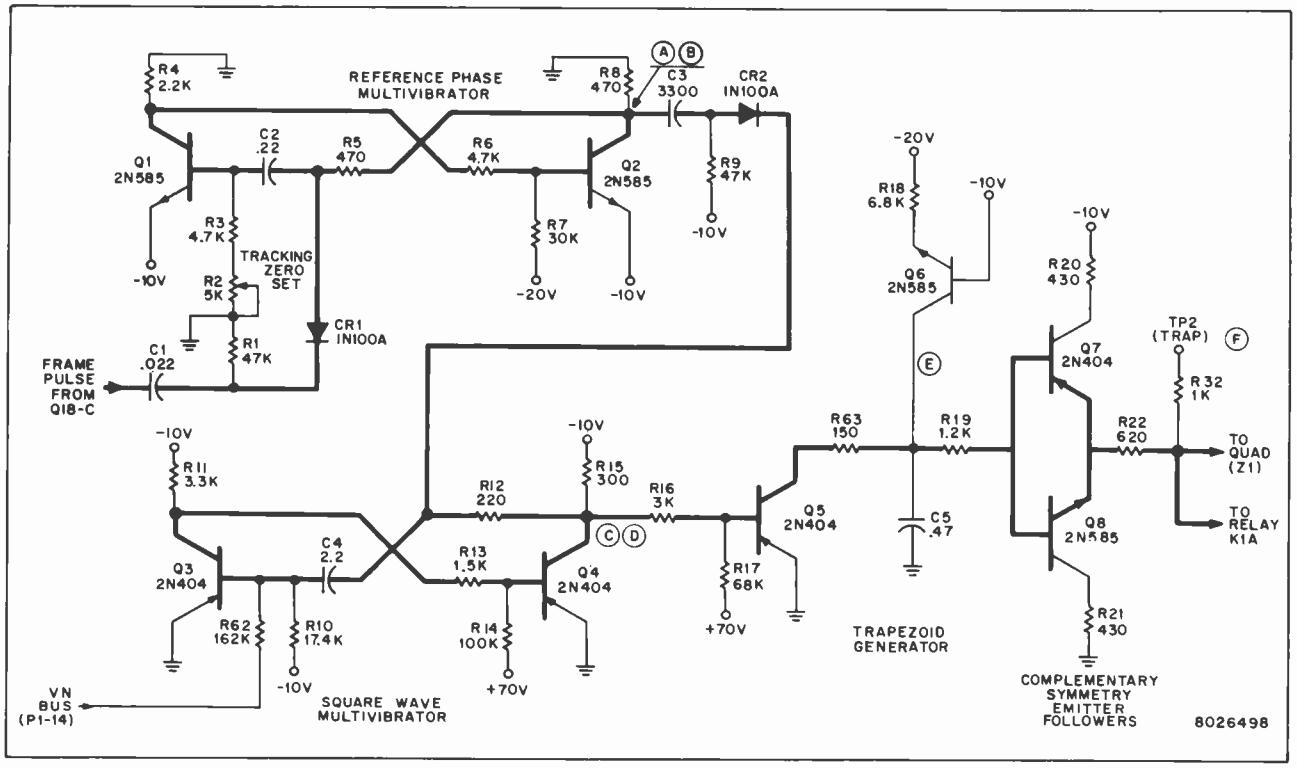
In the multivibrator stable state, transistor Q1 is biased into saturation while transistor Q2 is biased at cut-off. When the negative-going spike appears at the base of transistor Q1, the transistor is cut off. Transistor Q2 is simultaneously driven into saturation, and the output at its collector is then a negative-going pulse (figure 92A). The width of the negative-going pulse is determined by the time constant established as capacitor C2 charges through resistor R3 and potentiometer R2. The time constant, and thus the delay introduced, may be varied over a range of approximately 700 microseconds by adjusting potentiometer R2 (TRACKING ZERO SET). (The negative-going pulse at the collector of transistor Q2 is shown in figure 92B, top, with potentiometer R2 adjusted for minimum delay, and in figure 92B, bottom, with R2 adjusted for maximum delay.) The TRACKING ZERO SET control, located on the module front panel, is actually a fine adjustment of the control track phasing, and its purpose is to provide a means of exactly centering video head no. 1 over track no. 1 of a "standard" recording when the C.T. PHASE control (on the PLAY control panel) is at "0" position (see *Adjustments*). Diode CR1 disconnects the multivibrator from the triggering circuit during the timed interval so that the timing cycle cannot be influenced by leakage currents, and thus timing stability is improved.

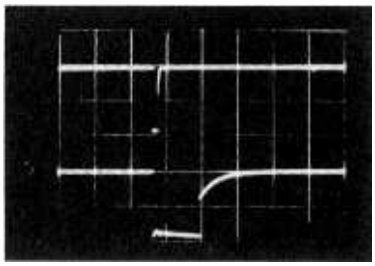
The negative-going pulse output at the collector of transistor Q2 is differentiated by the network consisting of capacitor C3 and resistor R9. The resulting positive-going spike, corresponding to the positive-going trailing (delayed) edge of the reference phase multivibrator output, is fed through diode CR2 to the base of transistor Q3. Transistors Q3 and Q4 combine to form the monostable square wave multivibrator and, in the multivibrator stable state, transistor Q3 is biased into saturation while transistor Q4 is biased at cut-off. The delayed positive-going spike fed to the base of transistor Q3 cuts the transistor off, thus beginning the multivibrator action.

When the machine is operated on 525-line (domestic) standards, the VN bus potential is −20 volts dc. During the multivibrator "off" time then, capacitor C4 charges through resistor R10 returned to −10 volts, and through resistor R62 returned to −20 volts. This results in a duty cycle which insures that the multivibrator recovery time is short enough to allow the multivibrator to be triggered by the 30-cycle triggering pulse which occurs when external servo reference is used, but is too long to permit triggering at the 60-cycle rate which occurs when the machine is operated with line servo reference. Thus when line servo reference is used, the multivibrator is triggered by every second pulse and a divide-by-two action is effectively obtained. Therefore, regardless of whether the machine is operated with external or line servo reference, the output at the collector of transistor Q4 is a 30-cycle square wave (figure 92, C and D) during tape playback on 525-line standards. Diode CR2 functions similarly to diode CR1; i.e., it disconnects the square wave multivibrator from the triggering circuit during the timed interval so that timing stability will be improved.

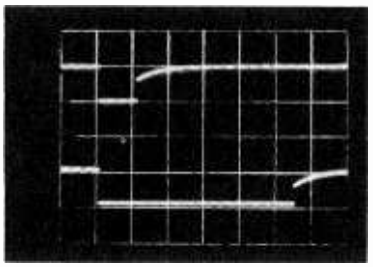
When the machine is operated on any of the International standards, the VN bus is at ground potential and thus resistor R62 is returned to ground. This effectively lengthens the multivibrator recovery time so that 25-cycle triggering pulses will produce a 25-cycle square wave when the machine is operated with external servo reference. Again, the duty cycle will be too long to allow the multivibrator to be triggered by the 50-cycle triggering pulse which occurs when the machine is operated with line servo reference, and the divide-by-two action results. Therefore, the output at the collector of transistor Q4 will always be a 25-cycle square wave signal during tape playback on any of the International standards.

Transistors Q5 and Q6 in conjunction with associated circuit components form the trapezoid generator circuit. Transistor Q5, normally saturated, is driven into cut-off by the positive portion of the square

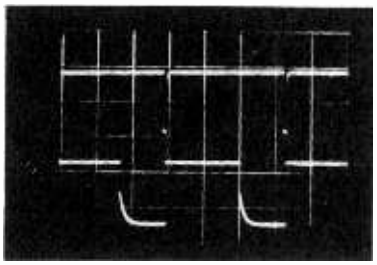




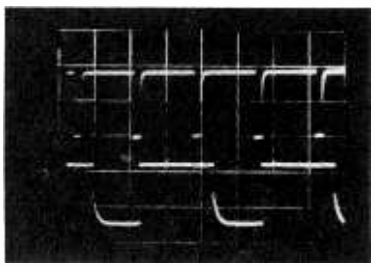
A. Top: TP1 (REF FRAME).
Bottom: Q2 collector (R2 correctly adjusted).
(500 μsec/cm)



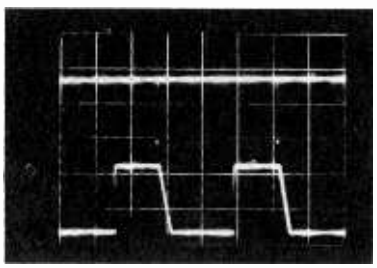
B. Top: Q2 collector (R2 adjusted for minimum), 10v/cm.
Bottom: Q2 collector (R2 adjusted for maximum), 10v/cm.
(500 μsec/cm)



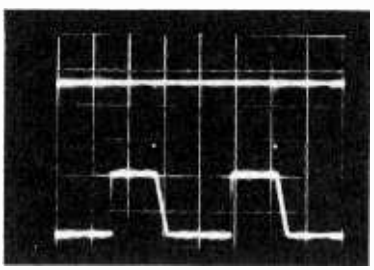
C. Top: Q2 collector.
Bottom: Q4 collector.
(EXT Servo Reference)



D. Top: Q2 collector.
Bottom: Q4 collector.
(LINE Servo Reference)



E. Top: TP1 (REF FRAME).
Bottom: Q6 collector.



F. Top: TP1 (REF FRAME).
Bottom: TP2 (TRAP).

Machine in PLAY mode. All sweep times 10 msec/cm and amplitudes 5v/cm, unless otherwise noted.

Figure 92—Reference Trapezoid Generator

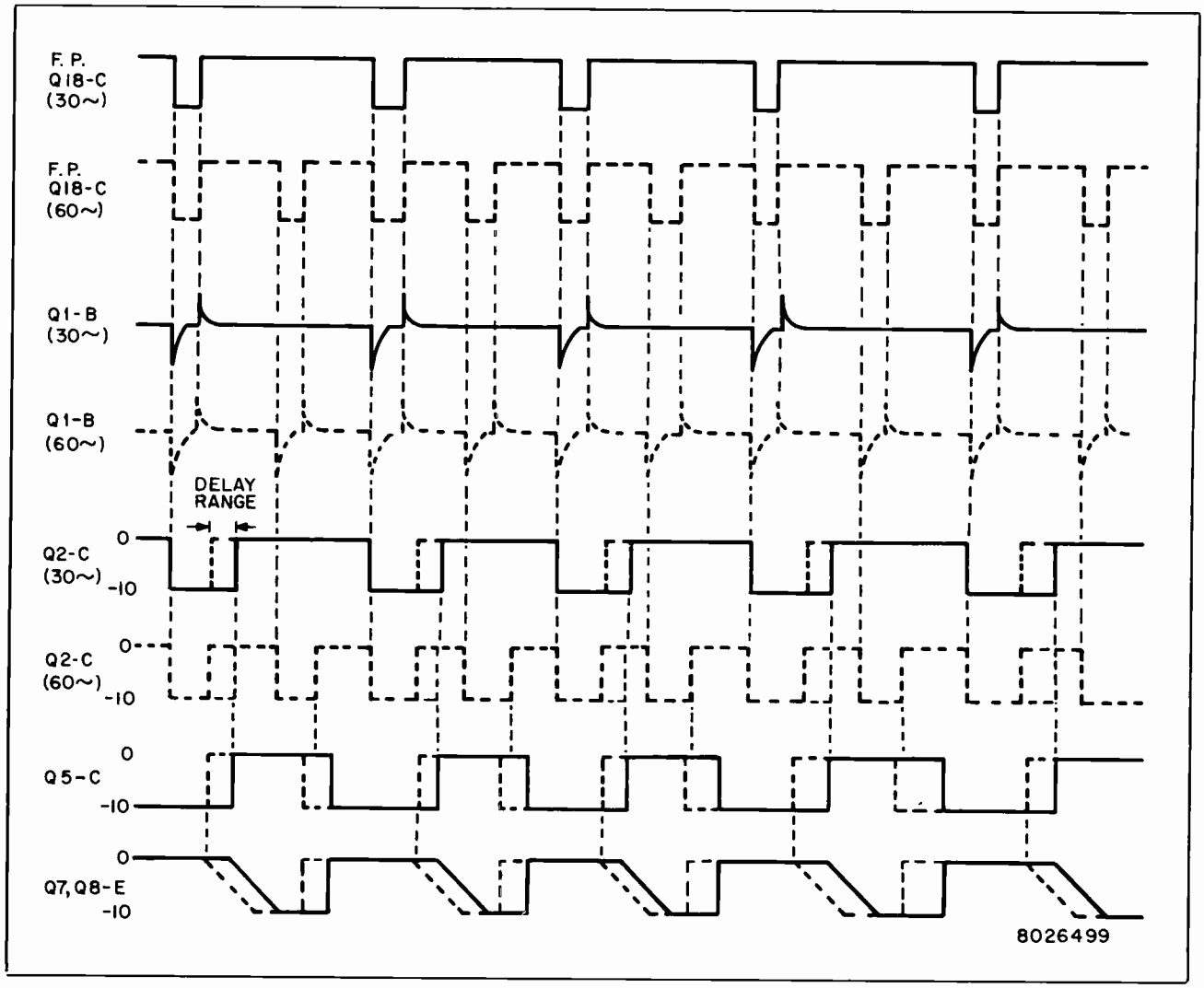
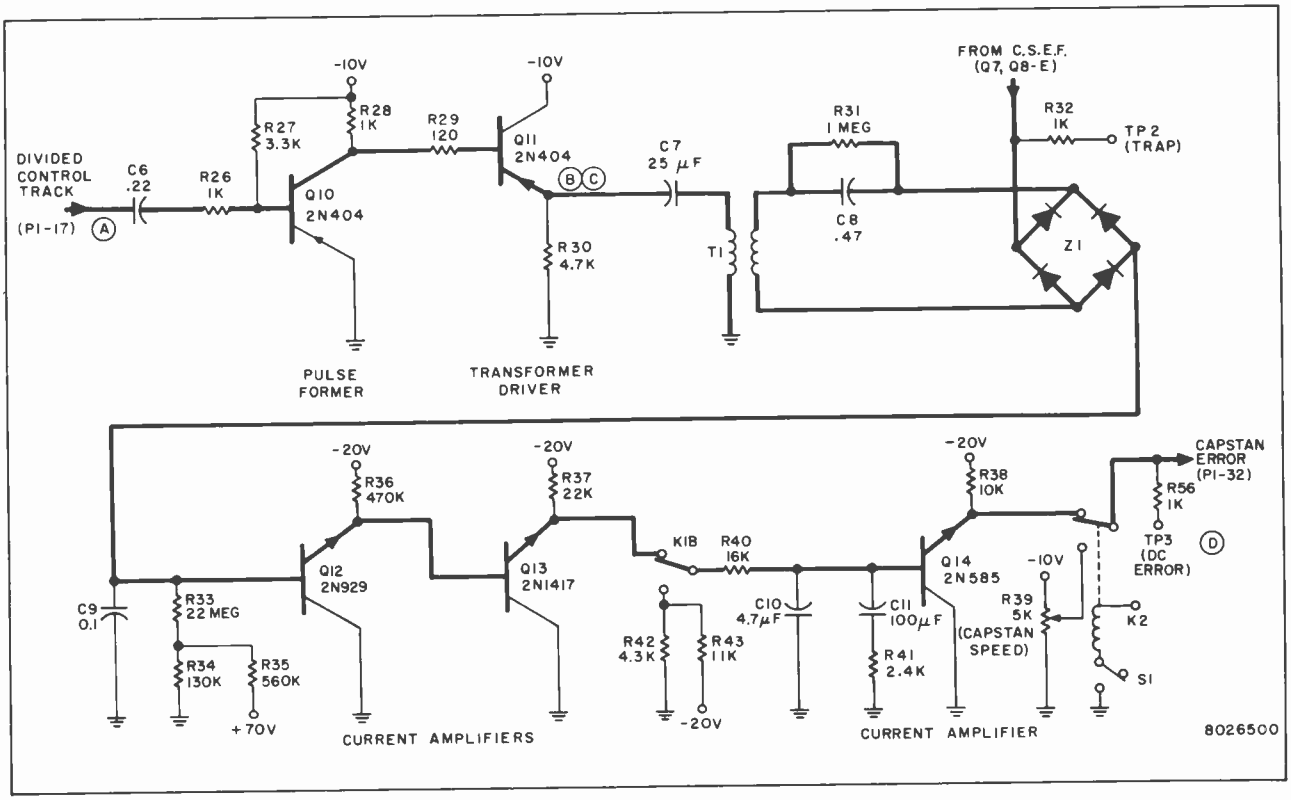
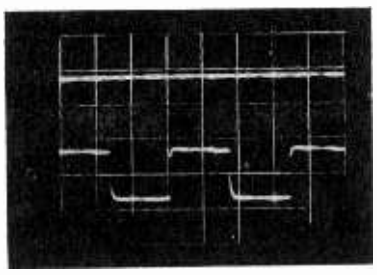


Figure 93—Reference Trapezoid Generator Timing Diagram

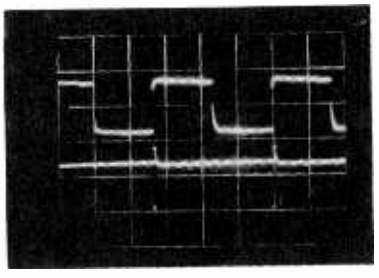
wave output at the collector of transistor Q4. When transistor Q5 is cut off, capacitor C5 charges from ground potential to a maximum of −10 volts and holds this voltage until Q5 is driven into saturation. The charging path of capacitor C5 is through resistor R18 and the constant current source transistor Q6, which is biased "on" when its collector voltage is more positive than −10 volts. The charging rate of capacitor C5 defines the slope of the trapezoid waveform, and is determined by the value of resistor R18 (6800 ohms). This value has been found to result in maximum allowable servo gain without objectionable capstan motor overcorrection or "hunting" (see *Comparator Bridge Circuit* description below). When transistor Q5 is driven into saturation by the negative portion of the square wave applied to its base, capacitor C5 discharges very rapidly through Q5 and the 150-ohm current limiting resistor R63. Thus the discharge time of capacitor C5 is short when compared with the period of the trapezoid waveform.

The resulting trapezoid waveform (figure 92E) is fed simultaneously to the bases of transistors Q7 and Q8 which form the complementary symmetry emitter follower circuit. The purpose of this circuit is to lower substantially the trapezoid generator output impedance to prevent any loading effect by the circuits which follow. From the common emitter circuit of transistors Q7-Q8, the trapezoid waveform is fed to the phase comparator bridge circuit (see description below) and the normally closed contact of relay K1. (The operation of relay K1 is described below under *CRO Driver Circuit.*) Test point TP2 (TRAP) is provided for convenience in observing the reference trapezoid waveform, which is shown in figure 92F.

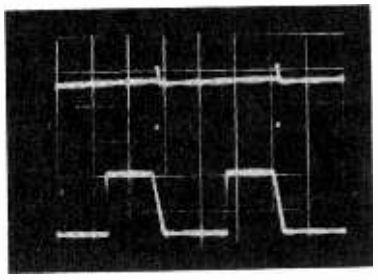




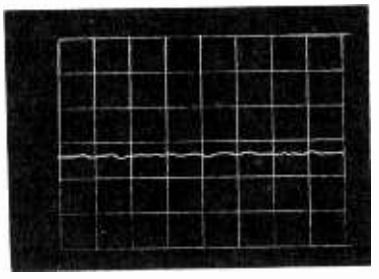
A. Top: TP1 (REF FRAME). Bottom: P1-17 (Divided Control Track).



B. Top: P1-17 (Divided Control Track). Bottom: Q11 emitter.



C. Top: Q11 emitter. Bottom: TP2 (TRAP).



D. TP3 (DC ERROR), 0.5v/cm. (500 msec/cm)

Machine in PLAY mode. All sweep times 10 msec/cm and amplitudes 5v/cm, unless otherwise noted.

Figure 94—Sample Pulse Generator and Comparator Bridge Circuit

Sample Pulse Generator and Comparator Bridge Circuit

The sample pulse generator circuit (figure 94) receives the divided-down control track signal from the capstan phase module (no. 320) and forms it into a clamp (sample) pulse, which is then applied to the phase comparator bridge. The reference trapezoid waveform, generated as described above, is also fed to the comparator bridge and is sampled during each cycle by the application of the sample pulse to the bridge. When the capstan motor speed is approximately correct, the sample pulse samples on the slope of the trapezoid waveform and the instantaneous trapezoid voltage during the sampling interval forms the error signal used by the capstan oscillator (in module no. 322) in obtaining the exact capstan motor speed.

The 30-cycle square wave (25-cycle in International machines) representing the divided-down control track signal, is fed through pin 17 of plug P1 to the pulse narrowing "boxcar" circuit of transistor Q10 (figure 94A). Transistor Q10, normally saturated, is driven into cut-off by the positive-going edge of the incoming square wave and, since the square wave amplitude is approximately 5 volts, the base potential of Q10 rises to approximately +4.8 volts. As capacitor C6 charges through current limiting resistor R26 and resistor R27 returned to −10 volts, the base potential of transistor Q10 increases in a negative direction. When the base potential reaches a point which is slightly negative with respect to ground, transistor Q10 is again driven into saturation. This action results in a negative-going output pulse, having a width which is determined by the values of capacitor C6 and resistors R26, R27, at the collector of transistor Q10. Emitter follower transistor Q11 provides the negative-going sample pulse with sufficient current gain, at a low impedance, to drive pulse transformer T1. The sample pulse at the emitter of transistor Q11 is shown in figure 94, B and C.

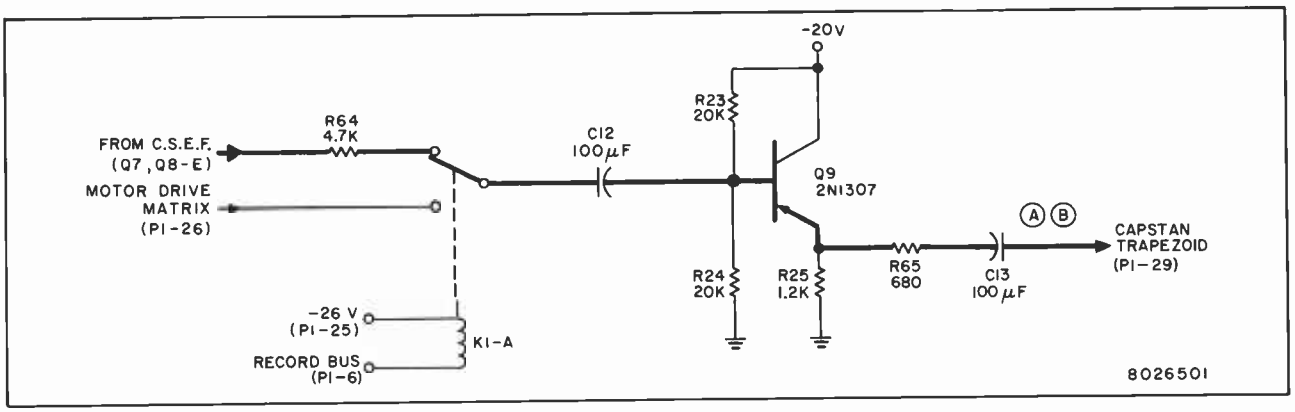
Quad Z1 forms the phase comparator bridge, whose diodes are normally biased so that the quad is cut off (open). When a sample pulse is fed from the emitter of transistor Q11 to transformer T1, the transformer splits the phase of the pulse so that opposite ends of the quad are driven simultaneously by pulses of opposite polarity. This action closes the quad and the output voltage from the complementary symmetry emitter follower transistors Q7-Q8 will be fed directly to storage capacitor C9, which rapidly charges to a voltage level corresponding to the voltage on the trapezoid slope at the instant the sample pulse occurs. After the sample pulse has occurred the quad is again cut off and, because of the relatively long RC time constant formed by capacitor C9 and resistors R33, R34, the capacitor will retain most of its charge until the next sample pulse occurs. Thus capacitor C9 stores or "remembers" the error until the next data sample is received.

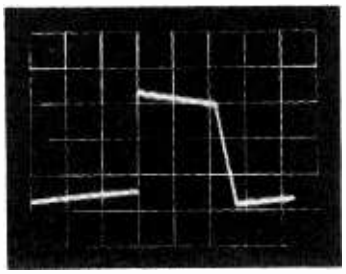
In the PLAY mode then (relay K1 deenergized) the error signal appearing across capacitor C9 is fed to emitter follower transistors Q12, Q13, and Q14 in cascade. These transistors isolate the quad from the output circuit and provide the current gain necessary to drive the oscillator control circuits in the capstan oscillator module. Capacitors C10, C11 and resistors R40, R41 in the base circuit of transistor Q14 form an anti-hunt network whose purpose is to stabilize the overall servo loop by controlling the high frequency response. The component values chosen control amplitude and phase response characteristics of the servo loop so that it is possible to operate the servo at higher overall d-c gain and thus obtain "tighter" servoing. The d-c error signal output shown in figure 94D, is fed via relay K2 and pin 32 of plug P1 to the capstan oscillator module (no. 322) and may be observed at test point TP3 (DC ERROR).

The capstan speed control (CAPSTAN SPEED) on the module front panel is a combined switch (S1) and potentiometer (R39). When the switch is turned "on", the coil of relay K2 is grounded and thus the relay is energized. This opens the d-c error output from the capstan servo loop and allows the capstan motor to be controlled manually by potentiometer R39 during tape playback. As mentioned above in the *General* description, the purpose of this control is to synchronize two tape machines which are playing back identical tapes simultaneously. Switch S1 is spring-loaded and during normal playback operation will be "off" so that the capstan motor will be controlled by the servo.

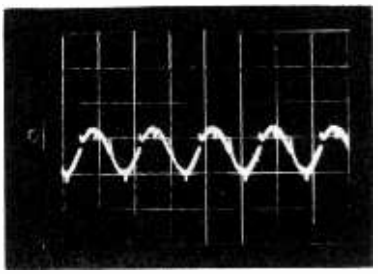
CRO Driver Circuit

When the machine is operated in the PLAY mode, relay K1 is deenergized and the trapezoid waveform is fed from complementary symmetry emitter follower transistors Q7-Q8 to emitter follower transistor Q9 in the CRO driver circuit as well as to the comparator bridge circuit (figure 95). Transistor Q9 provides sufficient current gain, at a low impedance, to drive the CRO monitor. The output at the emitter of Q9 is fed from pin 29 of plug P1 to the CRO monitor switcher, and may be observed on the CRO monitor by pressing the CAP SERVO pushbutton on the switcher. Resistor R65 is inserted into the output path to lengthen the RC time constant (R65, R25, C13) so that the waveform presentation on the monitor, which has an input termination of 75 ohms, will not





A. P1-29 (PLAY mode), Capstan Trapezoid, 0.2v/cm. (5 msec/cm)



B. P1-29 (RECORD mode), Motor Drive Matrix, 0.1v/cm. (10 msec/cm)

Figure 95—CRO Driver Circuit

be distorted. Figure 95A shows the trapezoid waveform which will be observed on the monitor during tape playback with the capstan servo properly locked. (Note that a pip corresponding to the sample pulse appears on the slope of the trapezoid waveform. This is due to a slight interaction between the sample pulse and trapezoid generating circuits which is intentionally introduced so that it is possible to monitor the servo action.)

In the RECORD mode the RECORD bus, and thus pin 6 of plug P1, is at ground potential. This energizes relay K1 so that the motor drive sine wave, fed to the module through pin 26 of plug P1 from the capstan oscillator module, will be applied to the CRO driver circuit during the RECORD mode. Transistor Q9 operates as described in the paragraph above, and the sine wave output, shown in figure 95B, may be observed on the CRO monitor when the CAP SERVO pushbutton on the CRO monitor switcher is depressed.

Adjustments

The purpose of the TRACKING ZERO SET screwdriver adjustment is to provide a means of exactly centering video head no. 1 over the track containing vertical sync of a "standard" tape when the C.T. PHASE control on the PLAY panel is set at "0" position during tape playback. The following procedure presents an efficient method of obtaining the correct adjustment:

1. Play back a standard test tape with the selector switch on the TAPE SYNC PROC module (no. 317) in TW position.

2. Place HEAD SELECT switch on reference generator module (no. 312) in position 1.

3. Press SW OUT pushbutton switch on CRO monitor switcher and rotate C.T. PHASE control on the PLAY control panel until head no. 1 is playing back the track containing vertical sync. (This may be determined by noting a sharp increase in amplitude of the rf band containing vertical sync when the CH ID pushbutton on the PB AMP 1 module, no. 215, is depressed.)

4. Rotate C.T. PHASE control slowly toward "0" position, while simultaneously maintaining a peak rf band amplitude by varying the TRACKING ZERO SET screwdriver adjustment.

5. When the C.T. PHASE control has reached "0" position, peak the rf band amplitude with the TRACKING ZERO SET adjustment.

6. Make a final check by ascertaining that the machine will go into switchlock or pixlock servo mode as observed on the picture monitor with the monitor triggered by external sync.

CAPSTAN OSCILLATOR MODULE

Circuit Description

General

The capstan oscillator module (no. 322) converts a 240-cycle signal into two 60-cycle sine wave outputs which are fed to the capstan power amplifiers (module nos. 330 and 331) which in turn drive the capstan motor. (In International machines, the signals occur at a 250-cycle rate and are converted into 62.5-cycle sine wave outputs.) When the machine is operated in the PLAY mode, the 240-cycle signal is a square wave generated by a local oscillator within the module itself. The frequency of the oscillator is controlled by the error signal developed in the capstan error module (no. 321). When the machine is operated in the RECORD mode, the 240-cycle signal is the tonewheel pulse obtained from the tonewheel processor module (no. 313) via the FM switcher module (no. 318).

In either mode of machine operation, the 240-cycle signal is divided-down by a ÷2 binary counter, and the outputs from this counter are fed through parallel paths which include either the master binary counter or slave binary counter in addition to filter circuits and a phase amplifier. (See block diagram, figure 96.) The output signals from the ÷2 binary counter occur at a 120-cycle rate and are 180 degrees out of phase. Each signal is then divided once again by either the master or slave binary counter, and the accompanying phase division results in output signals which occur at a 60-cycle rate and differ in phase by 90 degrees.

Due to the nature of the capstan motor, it is necessary that a certain phase relationship be maintained between the 60-cycle sine wave outputs to insure motor rotation in the correct direction. This is accomplished by utilizing a diode gating circuit to control the phase of the slave binary so that its output signal will always lead that of the master binary by 90 degrees. Filter circuits convert the binary outputs from square wave to sinusoidal signals. The sinusoidal signals are then amplified to approximately 6 volts peak-to-peak and fed to the power amplifiers.

240-Cycle Oscillator

The 240-cycle oscillator used in the capstan servo system is a free-running square wave multivibrator which normally oscillates at approximately 240 cps (250 cps in International machines). During tape playback, the oscillator frequency is determined by the magnitude of the input error voltage obtained from the capstan error module (no. 321). This voltage is negative, and the oscillator frequency is directly proportional to the voltage amplitude; i.e., as the error voltage increases in a negative direction the oscillator frequency increases, and vice versa. In the RECORD mode, the capstan motor speed is controlled by the tonewheel pulse, thus "locking" the capstan motor speed to that of the headwheel motor, and the oscillator is disconnected from the capstan servo circuitry.

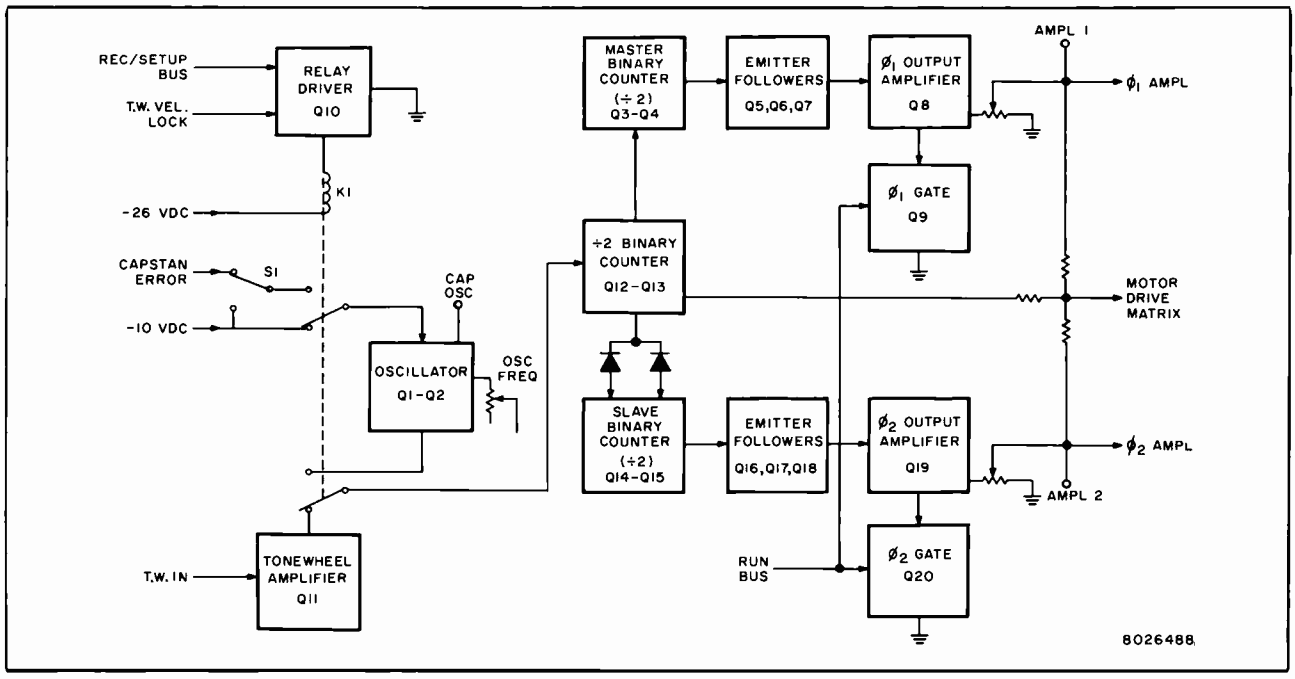
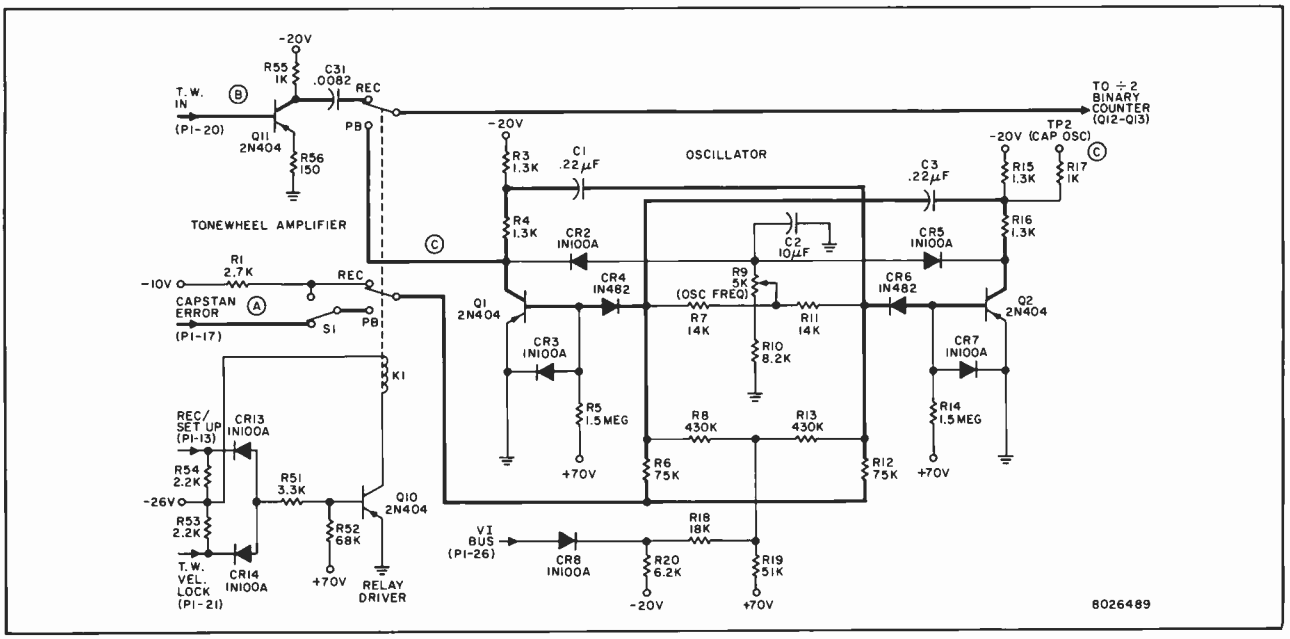
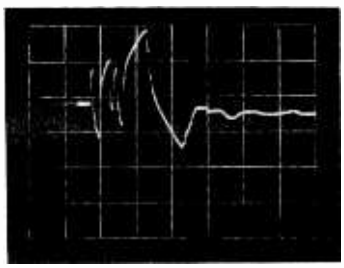
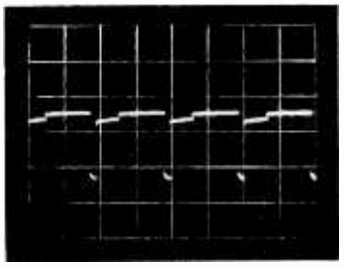


Figure 96—Capstan Oscillator Module Block Diagram

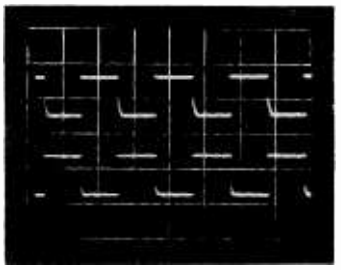




A. P1-17 (Capstan Error), 0.5v/cm. (500 msec/cm)



B. P1-20 (Tonewheel In), 2v/cm.



C. Top: Q1 collector, 10v/cm. Bottom: Q2 collector, 10v/cm.

Machine in PLAY mode. All sweep times 2 msec/cm, unless otherwise noted.

Figure 97—240-Cycle Capstan Oscillator

Selection of the tonewheel pulse (in the RECORD mode) or the 240-cycle oscillator output (in the PLAY mode) as a signal source, is determined by the relay K1 which in turn is controlled by the relay driver transistor Q10. When transistor Q10 is cut off, relay K1 is deenergized; when Q10 is saturated, the coil of K1 is returned to ground and the relay is energized. The condition of transistor Q10 is determined by the d-c potentials applied to the AND gate consisting of diodes CR13, CR14 and resistors R53, R54 (see figure 97). These potentials will be either −26 volts dc or ground, depending upon the mode of tape recorder operation and upon whether or not the headwheel motor is "locked-in" at the proper speed.

In the PLAY mode of operation, the REC/SU bus is at −26 volts dc. This potential is applied to the module through pin 13 of plug P1 and thus appears at the intersection of diode CR13 and resistor R54. Diode CR13 is forward biased by the negative potential and diode CR14 is cut off. Therefore, regardless of the TW VEL LOCK potential applied to the module at pin 21 of plug P1, transistor Q10 will be biased into saturation by the voltage divider action of resistors R52 and R51 returned to +70 volts dc and −26 volts dc respectively. Relay K1 is thereby energized and the capstan error voltage (figure 97A) generated in the capstan error module (no. 321) is fed to the oscillator circuit which in turn controls the capstan motor speed.

In the RECORD mode, the REC/SU bus is at ground potential; however, the TW VEL LOCK potential (obtained from the tonewheel servo module, no. 314) is −26 volts until the headwheel motor "locks in" at the proper speed. While the TW VEL LOCK potential is at −26 volts, diode CR14 is forward biased and diode CR13 is cut off. Thus transistor Q10 is again biased into saturation and relay K1 is energized. When the headwheel motor attains a servo

"lock", the intersection of diode CR14 and resistor R53 is at ground potential. Since the REC/SU bus is also at ground potential, the voltage distribution through the divider network (R52, R51) shifts so that a positive potential is applied to the base of transistor Q10, thereby cutting the transistor off. Relay K1 is then deenergized, thus disconnecting the oscillator circuit and allowing the capstan motor speed to be controlled by the tonewheel pulse (figure 97B).

From the above description of the relay and relay driver circuit, it is evident that the moment the machine is turned "on" relay K1 is energized and, if the MASTER RECORD pushbutton is then pressed, the relay will remain energized until the headwheel motor attains its correct speed. Since the time required for the headwheel motor to reach the correct speed is very short, the relay becomes deenergized almost immediately and the module is prepared for operation in the RECORD mode. This slight time lag is a protective feature which prevents the low frequency signals which occur during headwheel motor "start-up" from being fed through the low-pass filter stages and phase amplifier circuits to the capstan power amplifier and the capstan motor. (If the start-up signals were not suppressed, they would cause excessive motor and power amplifier circuit currents to flow.)

Transistors Q1-Q2 and associated circuit components form the free-running multivibrator which oscillates at a nominal frequency of 240 cps (250 cps in International machines). The multivibrator circuitry is symmetrical, having two timing circuits with identical time constants, and the output is thus a symmetrical square wave. The following paragraphs, in conjunction with figure 97, explain the operation of the multivibrator circuit during tape playback:

In the multivibrator circuit, at any given instant one of the transistors will be saturated and the other will be cut off. Assuming transistor Q1 to be saturated, the collector potential of transistor Q2 will then be −20 volts and the base of Q1 will be at ground potential. This allows capacitor C3 to charge to −20 volts with respect to the base of transistor Q1. As transistor Q2 begins to conduct, due to the negative error voltage applied to its base, its collector immediately rises to ground potential and the potential at the junction of resistors R15 and R16 is −10 volts. Since the voltage across capacitor C3 cannot change instantaneously, the potential at the junction of diode CR4 and resistor R7 will be forced to +10 volts (i.e., capacitor C3 is still charged to −20 volts with respect to the base of transistor Q1). Diode CR4 is cut off by the positive potential at its cathode, thus disconnecting the base of transistor Q1 so that as Q1 is driven into cut-off, its base leakage currents are isolated from the timing circuit. Diode CR3 is then forward biased by the +70 volt potential returned to ground through resistor R5 and the diode. Thus diode CR3 prevents the full +70 volt potential from being applied to the base of transistor Q1, while the small voltage drop across the diode (approximately 0.2 volt) is sufficient to hold the transistor in cut-off. When transistor Q1 is cut off, its collector potential begins falling toward −20 volts. As this potential reaches −10 volts, capacitor C1 begins to charge toward −20 volts through resistor R3 and the collector potential of transistor Q1 continues to decrease, although more slowly, toward −20 volts. While the collector potential of transistor Q1 is falling toward −20 volts, transistor Q2 is saturated and its base is thus essentially at ground potential.

Transistor Q1 will remain cut off as long as the potential on its base remains positive. However, the positive potential is due to the +10 volt charge on capacitor C3 (with respect to the base of transistor Q1), and at the instant Q1 is cut off, capacitor C3 begins to discharge through resistor R7 toward the negative potential at the center-arm of potentiometer R9. At the instant the voltage on capacitor C3 goes slightly negative, transistor Q1 will be driven into conduction and the capacitor will be clamped at ground potential.

Returning to the operation of the timing circuits, it may be seen in figure 97 that one end of the voltage divider network consisting of resistor R10 and potentiometer R9 is connected to the collector of either transistor Q1 or Q2 through diode CR2 or CR5 respectively, depending upon which diode is forward biased into conduction. Forward bias is applied to the diode associated with whichever transistor is cut off and, since during normal operation only one transistor at a time is cut off, only one of the diodes will conduct at any given instant. Therefore, one end of the voltage divider is always connected to the collector of the transistor which is cut off, and the potential at that end of the divider consequently remains at a level of approximately −17 volts, as determined by the applicable voltage divider network (e.g., R3, R4, R9, and R10 returned to ground). Any rapid potential changes or fluctuations are absorbed by capacitor C2.

The charging of capacitor C3 then, from +10 volts toward the negative potential at the center-arm of potentiometer R9, establishes the time interval of one half of the total multivibrator period. The second half of the period begins at the instant transistor Q1 conducts, and the sequence of operation is identical to that described above for the first half-period. The

frequency of operation is inversely proportional to the sum of the two half-periods and, if potentiometer R9 (OSC FREQ) is adjusted correctly (see *Adjustments*), the frequency of the oscillator will be 240 cps when the d-c error signal is at a constant, normal level.

When the incoming error signal varies in amplitude, actual control of the oscillator frequency is obtained by means of the current fed to the base circuits of transistors Q1 and Q2 through resistors R6 and R12 respectively. This method of frequency control introduces a current into the oscillator charging circuits (C3, R7 and C1, R11) which is proportional to the amplitude of the error signal deviation from its normal level. The injected current modifies the normal charging currents, thereby altering the rate at which the capacitors (C3 and C1) charge toward the potential at the center-arm of potentiometer R9. As the charging rate of each capacitor varies, the period of the multivibrator (and therefore the frequency of oscillation) changes. By utilizing this method of frequency control, any deviation in the d-c error signal amplitude from its normal value (due to errors in tape speed) will alter the oscillator frequency, thereby causing a corresponding correction in the capstan motor speed so that the error is continually held at a minimum by the servo action.

The above discussion assumes machine operation on 525-line (domestic) standards. In this case the VI bus, and thus pin 26 of plug P1, is at ground potential and diode CR8 is forward biased. This results in a positive current being fed through a 430K ohm resistor to whichever timing circuit is in operation, thereby lengthening the time constant slightly to obtain the desired 240-cycle oscillation. When the machine is operating on International 625-line standards, the voltage at the anode of diode CR8 is −20 volts dc and the diode is cut off. This shifts the potential at the junction of resistors R18 and R19 in a negative direction, thereby shortening the recovery time of each half of the multivibrator to obtain oscillation at a 250-cycle rate.

The square wave signal at the junction of resistors R15 and R16 in the collector circuit of transistor Q2 is shown in figure 97C, and may be observed at test point TP2 (CAP OSC) which is provided as a convenient observation point for determining whether or not the multivibrator is operating normally. The square wave output at the collector of transistor Q1 (figure 97C) triggers the ÷2 binary counter Q12-Q13 (see *Binary Counter Circuit* description below). Switch S1, a momentary contact pushbutton type located on the module front panel, opens the error signal path when depressed and allows a steady negative current, which approximates the normal error current in magnitude and direction, to flow into the multivibrator timing circuits from the junction of resistors R1 and R2. The switch is used in conjunction with the OSC FREQ screwdriver adjustment when setting the oscillator frequency with the machine operating in the PLAY mode (see *Adjustments*).

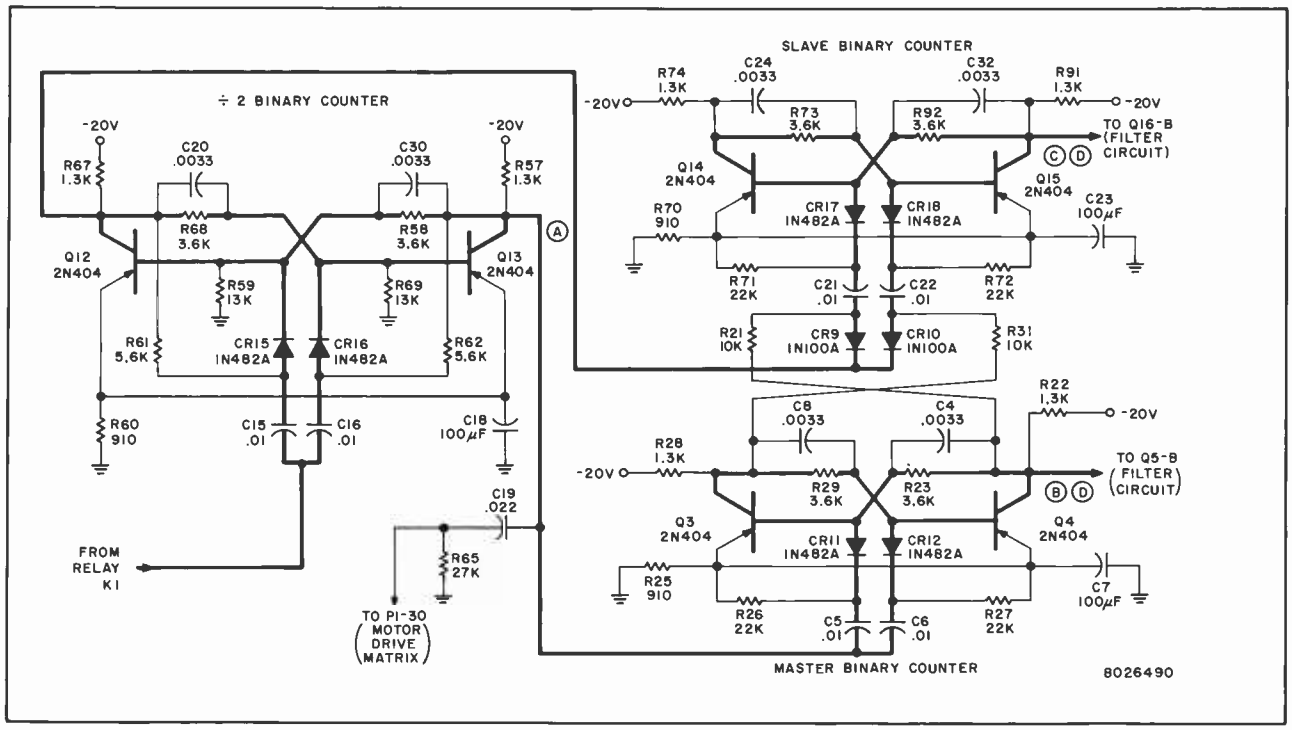
In the RECORD mode, the multivibrator circuit is not used. However, the same current which flows into the multivibrator timing circuits during tape playback with switch S1 depressed also flows when the machine is operating in the RECORD mode, regardless of the condition of S1. This arrangement prevents the oscillator frequency from drifting over a very wide range, and maintains the frequency at approximately 240 cps (250 cps on International standards) so that when the machine is switched to the PLAY mode, the frequency will be very close to the correct value (i.e., well within the servo "pull-in" range, so that oscillator "lock-out" is impossible).

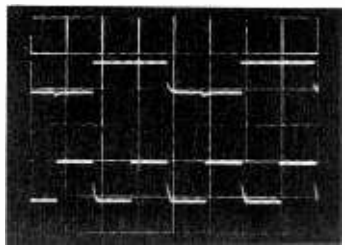
Binary Counter Circuits

The binary counter circuits (figure 98) divide-down the frequency and phase of the output signal from either the 240/250-cycle oscillator or the tonewheel amplifier circuit (depending upon the tape recorder mode of operation), and furnish two 60-cycle square wave signals, 90 degrees out of phase, to the filter and phase amplifier channels. Figure 99 shows the timing relationships between the 240-cycle input signal to the ÷2 binary counter, and the outputs from the master and slave binary counters.

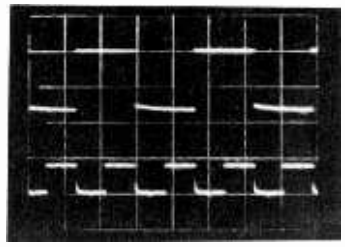
The ÷2 binary counter, consisting of transistors Q12, Q13 and associated circuit components, is a bistable device in which the transistors are d-c coupled. Therefore, either transistor will continue to conduct, while the opposite transistor remains cut off, until the state is reversed by a positive-going triggering pulse which cuts off the conducting transistor. In the PLAY mode of tape recorder operation, the 240-cycle square wave output from the collector of transistor Q1 in the oscillator circuit is differentiated by the networks consisting of capacitor C15, resistor R61 and capacitor C16, resistor R62. The positive-going spikes resulting from the differentiation are fed simultaneously through diodes CR15 and CR16 to the bases of transistors Q12 and Q13 respectively.

Assuming transistor Q12 to be saturated and transistor Q13 to be cut off, the positive-going spike will have no effect on Q13 but will cut Q12 off. The collector potential of transistor Q12 then immediately falls to approximately −18 volts, and this potential is d-c coupled to the base of transistor Q13, thus driving the transistor into saturation. The transistors will

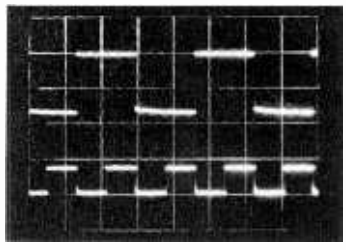




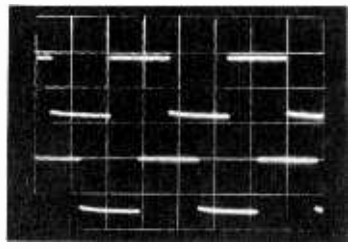
A. Top: Q13 collector, 10v/cm. Bottom: Q1 collector, 10v/cm. (2 msec/cm)



B. Top: Q4 collector, 5v/cm. Bottom: Q13 collector, 10v/cm.



C. Top: Q15 collector, 5v/cm. Bottom: Q12 collector, 10v/cm.



D. Top: Q15 collector, 5v/cm. Bottom: Q4 collector, 5v/cm.

Machine in PLAY mode. All sweep times 5 msec/cm, unless otherwise noted.

Figure 98—Binary Counters

remain in this state until the next positive-going spike occurs (corresponding to the positive-going edge of the 240-cycle square wave) and cuts off transistor Q13. The outputs at the collectors of transistors Q12 and Q13 will then be 120-cycle square wave signals differing in phase by 180 degrees as shown on the timing diagram (figure 99). "Speed-up" capacitors C20 and C30 (3300 μfd) assure more positive transistor switching so that the output square wave signals will have sharply defined timing edges. (Figure 98A shows the divide-by-two action of the multivibrator.)

When the machine is operated in the RECORD mode, the 240-cycle tonewheel pulse applied to the module through pin 20 of plug P1 is amplified by transistor Q11 and fed to the ÷2 binary counter

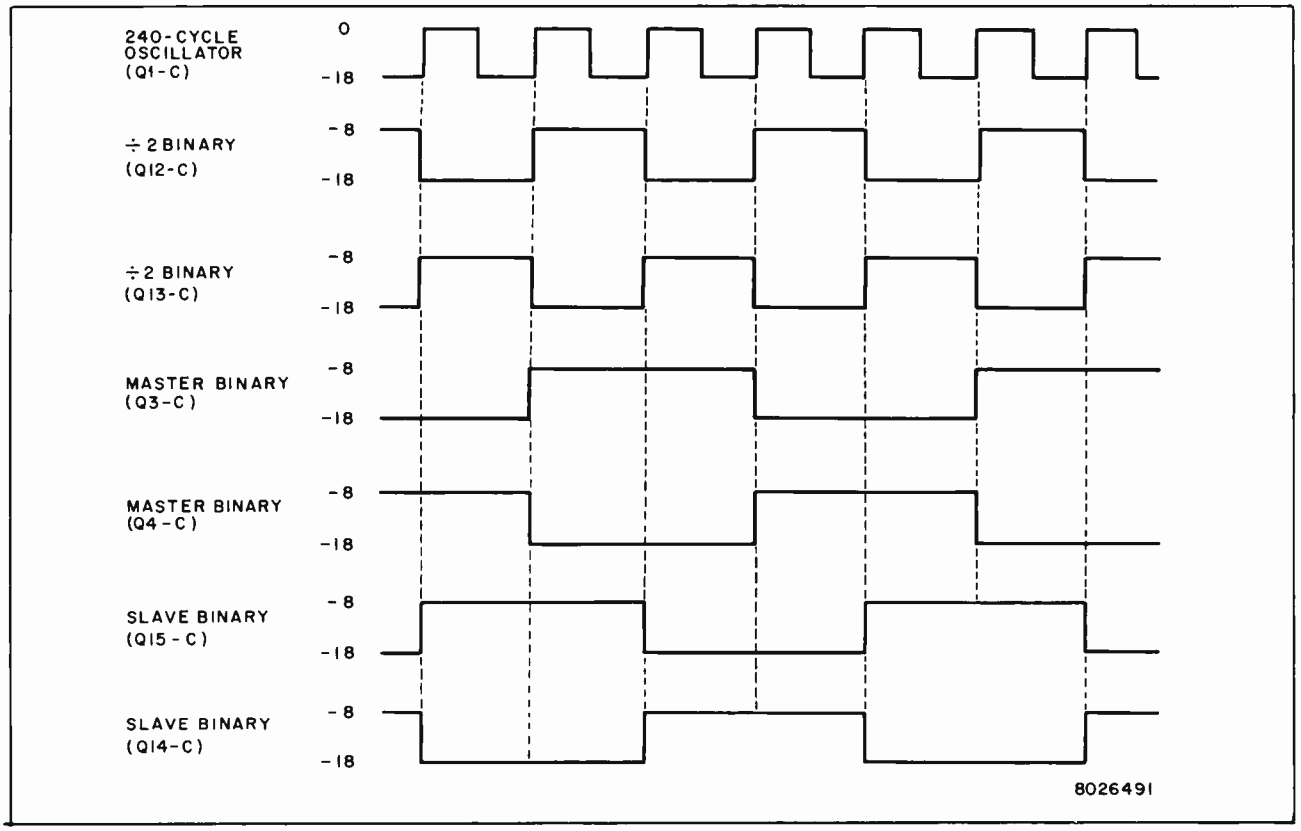


Figure 99—Binary Counter Waveform Timing Relationships

circuit. The amplified pulse is differentiated in the same manner as the 240-cycle square wave fed to the counter circuit from the oscillator during tape playback, and the counter then operates exactly as described above.

A differentiating network consisting of capacitor C19 and resistor R65 differentiates the square wave output at the collector of transistor Q13, and the resulting positive- and negative-going spikes (pips) are combined with the composite sine wave output from a matrixing network at pin 30 of plug P1 to form the motor drive matrix waveform (see *60-cycle Filter and Phase Amplifier* circuit description below).

The 120-cycle square wave signal at the collector of transistor Q13 is fed to the master binary counter circuit consisting of transistors Q3, Q4 and associated circuit components. The master binary counter, also a bistable device, operates similarly to the ÷2 binary counter with the exception that in the master binary counter circuit the non-conducting transistor is driven into saturation by the negative-going spike resulting from the differentiation of the 120-cycle square wave. Once again a divide-by-two action is attained, and the output signal at the collector of transistor Q4 is a 60-cycle square wave as shown in figure 98B. This signal is then fed to a filter network which converts it into a 60-cycle sine wave.

Coincidentally with the application of the 120-cycle square wave signal from the collector of transistor Q13 to the master binary counter, the 120-cycle square wave signal at the collector of transistor Q12 is fed to the slave binary counter, consisting of transistors Q14, Q15 and associated circuit components, through a diode gating circuit. Since it is not necessary to maintain a definite phase relationship between the outputs of the ÷2 binary counter and the master binary counter, the triggering of the master binary counter is random; however, to insure capstan motor rotation in the correct direction (clockwise), the output signal from the slave binary counter must lead that from the master binary counter by 90 degrees and for this reason the triggering of the slave binary counter must be controlled. Control is achieved through the use of a diode gating circuit comprised of diodes CR9, CR10 and resistors R21, R31, and the gating circuit in turn is controlled by the output signals at the collectors of transistors Q3 and Q4 in the master binary counter circuit. The following paragraphs, in conjunction with figure 100 and the timing diagram (figure 99), explain the gating circuit operation:

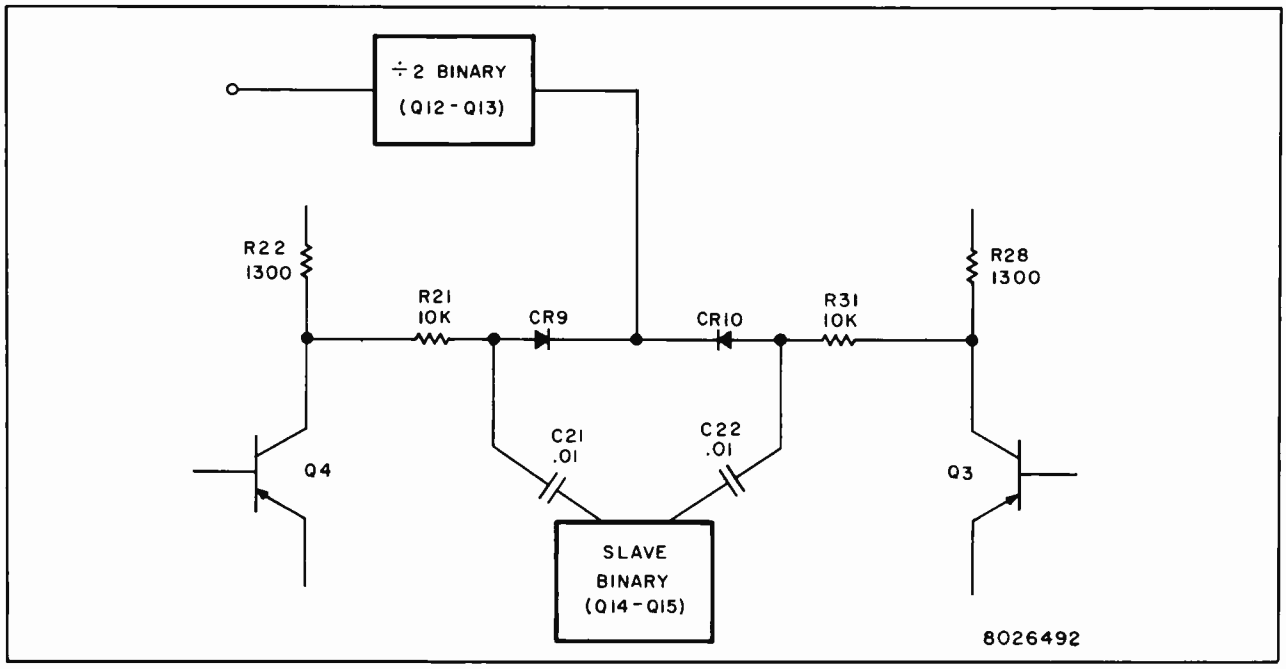


Figure 100—Phase-Locked Master/Slave Binary Counters

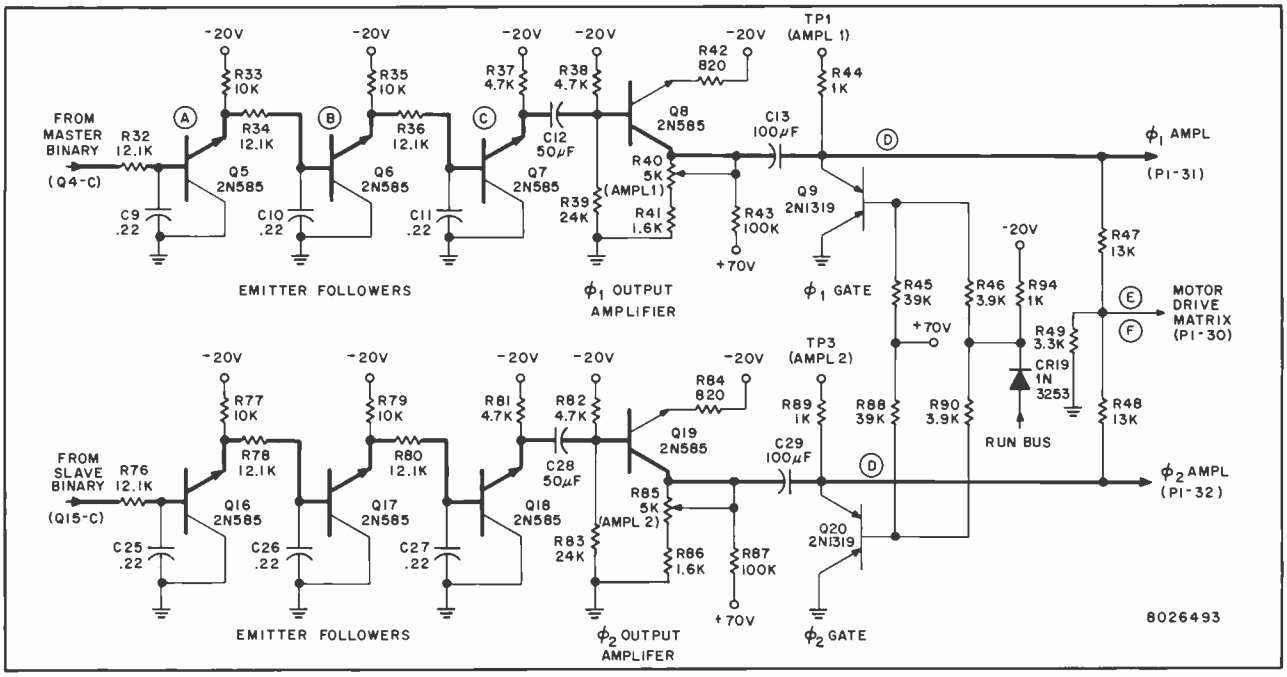
Assuming transistor Q3 to be saturated, its collector potential is then approximately −8 volts. This potential is fed through resistor R31 to the anode of diode CR10. However, the cathode of diode CR10 is driven by the 120-cycle square wave output from the collector of transistor Q12 and, since the square wave potential varies between the approximate limits of −8 and −18 volts, the diode will conduct and pass the square wave to the differentiating network of transistor Q15 in the slave binary counter circuit. Simultaneously, transistor Q4 is cut off and the potential at its collector falls to approximately −18 volts. This potential is applied to the anode of diode CR9 through resistor R21, thus cutting the diode off and blocking passage of the square wave to the differentiating network of transistor Q14. Since the slave binary counter circuit operates similarly to the master binary counter circuit except for the fact that its triggering sequence is controlled by the diode gate, the negative-going spike resulting from the differentiation of the square wave passed by diode CR10 will drive transistor Q15 into saturation.

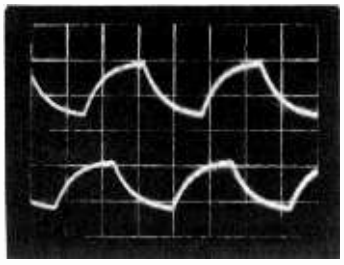
When transistor Q4 is saturated, the process is reversed and diode CR9 is biased into conduction while diode CR10 is cut off. The 120-cycle square wave signal is then fed to the differentiating network of transistor Q14 and the resulting negative-going spike drives Q14 into saturation. At the instant transistor Q14 is driven into saturation, transistor Q15 is cut off; however, since a time interval equal to one-half of the 120-cycle square wave period must elapse before transistor Q4 is again cut off, it is evident that the triggering of transistor Q15 leads that of transistor Q4 by an interval equal to one-half of the 120-cycle square wave period (i.e., one-quarter of a 60-cycle square wave period, or 90 degrees). This is clearly indicated in figure 98C and on the timing diagram (figure 99). The 60-cycle square wave output signal at the collector of transistor Q15 is then converted into a 60-cycle sine wave by a three-stage low-pass filter network. (Figure 98D shows the divide-by-two action of the slave binary counter.)

60-Cycle Filter and Phase Amplifier Circuits

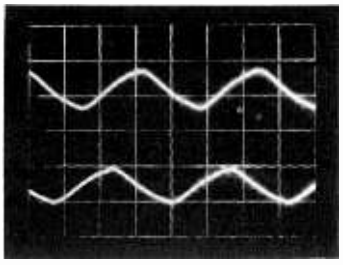
The 60-cycle square wave output at the collector of transistor Q4 in the master binary counter circuit is fed into a three-section low-pass filter network which converts the square wave into a relatively pure 60-cycle sine wave (figure 101). The filter sections, consisting of resistors R32, R34, R36, and capacitors C9, C10, C11, are coupled by emitter follower transistors Q5, Q6, Q7 to obtain impedance scaling. The emitter follower transistors provide an isolation ratio of approximately 25:1 between each resistance-capacitance section, thereby reducing the loading effect which each section presents to the preceding one. (Figure 101A, B, and C show the development of the 60-cycle sine wave.)

Transistor Q8, operating as a common emitter amplifier, amplifies the sine wave output from the filter circuit. The gain of the amplifier is determined

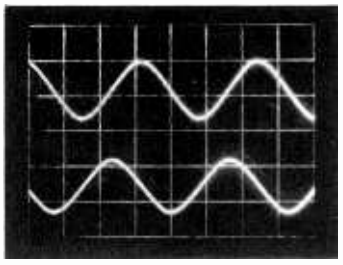




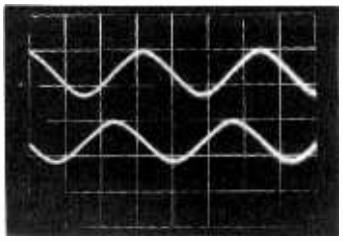
A. Top: Q5 base.
Bottom: Q16 base.



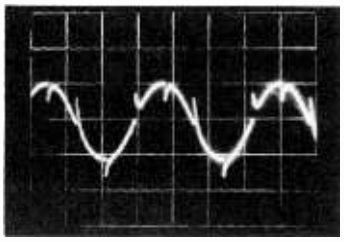
B. Top: Q6 base.
Bottom: Q17 base.



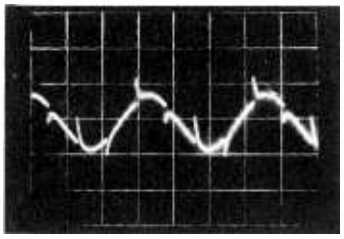
C. Top: Q7 base, 2v/cm.
Bottom: Q18 base, 2v/cm.



D. Top: TP1 (AMPL 1).
Bottom: TP3 (AMPL 2).



E. P1-30, Motor Drive Matrix (Normal Output), 0.5v/cm.



F. P1-30, Motor Drive Matrix (One Output Shorted), 0.5v/cm.

Machine in PLAY mode. All sweep times 5 msec/cm and amplitudes 5v/cm, unless otherwise noted.

Figure 101—60-Cycle Filter and Phase Amplifier Circuits

by the resistance ratio of resistor R41 and a portion of potentiometer R40 (depending upon the setting of the potentiometer) to resistor R42. Therefore, the amplitude of the 60-cycle sine wave output at the collector of transistor Q8 (ϕ_1 output) is determined by the setting of potentiometer R40 (AMPL 1). The potentiometer is normally adjusted to obtain an output signal amplitude of approximately 6 volts peak-to-peak (see *Adjustments*). This signal may be observed at test point TP1 (AMPL 1), and is shown in figure 101D (top).

An identical combination of circuits converts the square wave output from the collector of transistor Q15 in the slave binary counter circuit into an amplified 60-cycle sine wave. In order to preserve as closely as possible the 90 degree phase differential between the binary output signals, precision resistors are used in each resistance-capacitance filter section. The output

signal at the collector of phase amplifier transistor Q19 (ϕ_2 output) may be observed at test point TP3 (AMPL 2) and is shown in figure 101D (bottom).

When the machine is in the STOP mode, the RUN bus potential is −26 volts and diode CR19 is cut off. This places a negative bias voltage on the base of gating transistor Q9 from the voltage divider network consisting of resistors R45, R46, and R94, and the transistor is saturated. The output signal from phase amplifier transistor Q8 is then bypassed through transistor Q9 to ground. Simultaneously, gating transistor Q20 will be saturated, thus bypassing the output from phase amplifier transistor Q19 to ground. Therefore, when the machine is in the STOP mode, there will be no output voltage to the capstan power amplifiers and the capstan motor will not run. When the machine is in an operating mode (i.e., any mode except STOP), the RUN bus is at ground potential. This cuts off diode CR19 and causes the potential on the bases of the gating transistors to shift to a positive value which cuts the transistors off, thus allowing the motor drive signals to pass. The ϕ_1 output signal is then fed through pin 31 of plug P1 to capstan power amplifier no. 1 (module no. 330), and the ϕ_2 output signal is fed through pin 32 of plug P1 to capstan power amplifier no. 2 (module no. 331).

In addition to driving the power amplifiers, the ϕ_1 and ϕ_2 output signals are combined in the matrixing network consisting of resistors R47 and R48 to form a composite sine wave signal which leads the ϕ_1 output signal by 45 degrees and trails the ϕ_2 output signal by the same amount, and whose amplitude exceeds that of either output signal. The composite signal is then combined with the differentiated square wave output from the ÷2 binary counter to form the motor drive matrix waveform (figure 101E) which is fed through pin 30 of plug P1 to the capstan error module. This waveform has no significance during tape playback; however, when the machine is operated in the RECORD mode, the waveform is fed to the CRO driver circuit in the capstan error module and may be observed on the CRO monitor when the CAP SERVO pushbutton on the CRO monitor switcher is depressed.

When the machine is operating normally, in the RECORD mode, the phase relationships between the 60-cycle sine wave and 240-cycle pips will be as shown in figure 101E. (This waveform will be identical for the 62.5-cycle sine wave and 250-cycle pips obtained in International machines.) If the phase relationships are not as shown in figure 101E, the indication is that either the ϕ_1 or ϕ_2 output signal from the capstan oscillator module is missing (figure 101F). (The missing output signal may be easily detected by observing the waveform at the AMPL 1 and AMPL 2 test points.) If the pips are present in the waveform observed on the CRO monitor but the sine wave is not, the indication is that the ÷2 binary counter (driven by the tonewheel pulse) is operating correctly, however a failure in the succeeding circuitry is preventing the sine wave output from being supplied by the module. (The most likely cause of a failure of this type is a malfunction in the ϕ_1 and ϕ_2 gating circuit.)

Adjustments

Screwdriver adjustments are provided on the capstan oscillator module front panel for convenience in obtaining the correct oscillator frequency (240/250 cps) and the correct ϕ_1 and ϕ_2 output signal amplitudes (approximately 6 volts peak-to-peak). The values of these parameters should be checked at regular intervals and, if found to be incorrect, the procedures outlined below may be followed to obtain the correct values. If both gain and frequency adjustments are to be made, it is recommended that the gain adjustment be made first.

ϕ_1 and ϕ_2 Gain

1. Place the machine in SETUP mode.
2. Press the CM1 pushbutton (above the guide servo module) and note the voltage reading on the multimeter (below the picture monitor).
3. Vary the AMPL 1 screwdriver adjustment on the capstan oscillator module front panel to obtain a reading of 110 volts on the multimeter.
4. Press the CM2 pushbutton, and vary the AMPL 2 screwdriver adjustment to obtain 110 volts on the multimeter.

240/250-Cycle Oscillator

1. Play back a standard test tape on the machine.
2. Depress the CAP SERVO pushbutton on the CRO monitor switcher and, while pressing the momentary contact pushbutton switch on the capstan oscillator module, observe the motion of the pips on the slope of the trapezoidal waveform on the CRO monitor.
3. Vary the OSC FREQ screwdriver adjustment, with the momentary contact pushbutton switch pressed, to slow or stop completely the motion of the pips on the trapezoid slope.
4. Release pushbutton (the capstan should now "lock"), and obtain the proper phase relationship between pip and trapezoid waveform by varying the OSC FREQ adjustment slightly so that the pip is located approximately 40% up the trapezoid slope from the bottom (i.e., not at the center of the slope, or 50%).

VACUUM GUIDE SERVO

SYSTEMS DESCRIPTION

GENERAL

The function of the vacuum guide servo system, shown in simplified block diagram form in figure 102, is to control the position of the vacuum guide with respect to the rotating headwheel. The position of the guide is one of the factors determining the compatibility of playback between tapes which have been recorded by video heads whose degree of wear may vary from one machine to another. Thus the operation of the guide servo in maintaining the proper guide position during tape recording and playback is of great importance.

Essentially, the guide servo system consists of the guide servo module (no. 221), the guide actuating mechanism (located behind the headwheel panel), the playback pushbutton control switch (AUTO/MANUAL, located on the PLAY panel), and the guide position control utilized during tape recording (located on the RECORD panel). The guide servo module contains the electronic circuits which control the system, and the guide position control utilized during tape playback in manual mode is located on the module front panel. The guide actuating mechanism consists of a two-phase motor, coupled through reduction gears to the headwheel panel and the vacuum guide.

SYSTEMS ANALYSIS

Figure 103 shows a cross-sectional view of the vacuum guide and headwheel, indicating tape stretch due to indentation caused by the video magnetic heads. As the headwheel rotates, the video magnetic heads (protruding beyond the headwheel rim by approximately 1 to 3.4 mils, depending upon video head wear) cause the tape to stretch in a localized indentation which travels across the moving tape. This stretching of the tape is essential to correct for minor dimensional variations resulting from video head wear, differences in machines, and minute expansion or contraction of the tape. When recording, the guide is fixed at some position which is determined for the particular headwheel panel in use by the precise setting of the GUIDE POSITION control on the RECORD control panel. This insures the application of a constant pressure between the tape and the video heads, thus resulting in a fixed degree of tape stretch.

To attain optimum machine performance during tape playback, the relative head-to-tape speed must be held constant. The factors which determine the head-to-tape speed are the angular velocity of the headwheel and the position of the vacuum guide. The angular velocity of the headwheel is maintained at a constant value by the headwheel servo system; thus

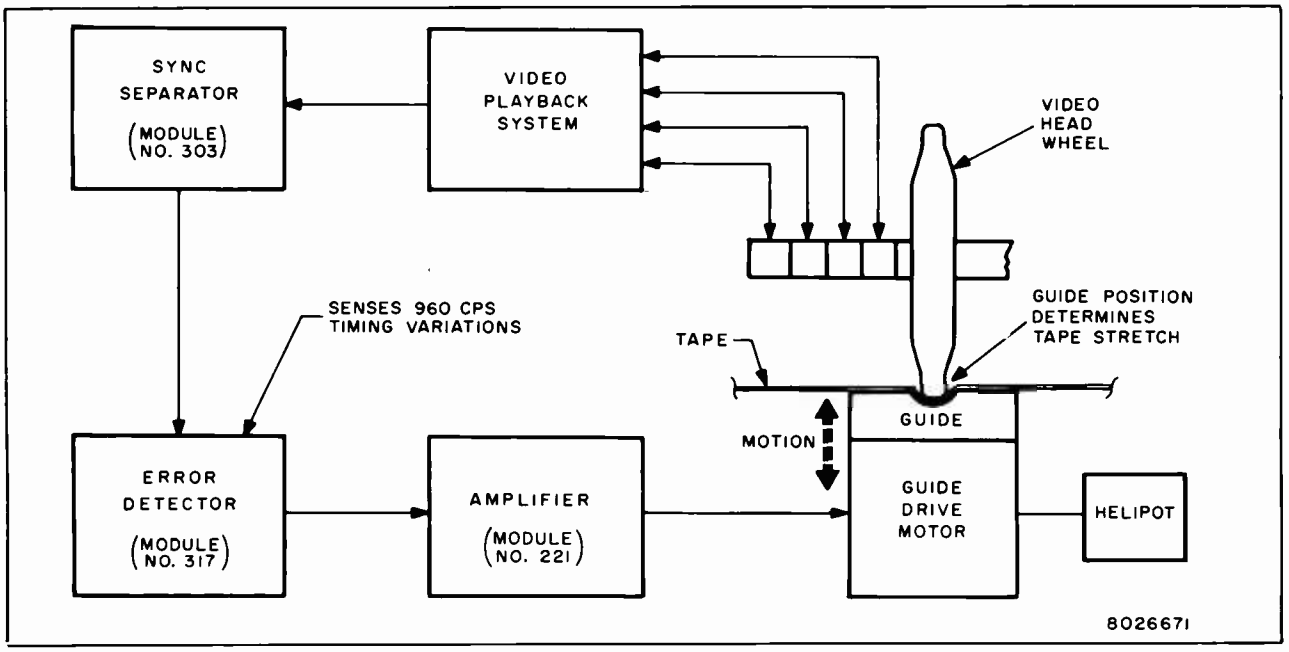


Figure 102—Simplified Block Diagram of Guide Servo System

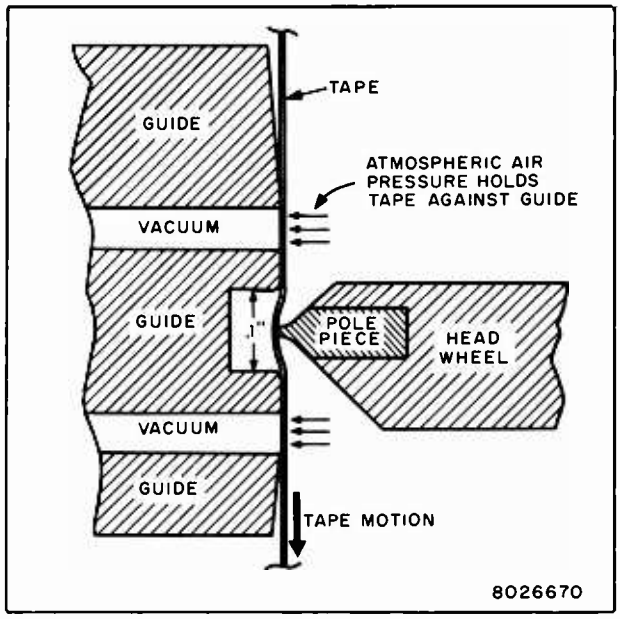


Figure 103—Cross-Sectional View of Vacuum Guide and Headwheel

angular timing errors are eliminated. However, unless the vacuum guide position is tightly controlled, timing errors will occur which cause certain geometric distortions in the picture. One form of geometric distortion is caused by time-displacement errors which appear in the form of discontinuities at the instant of video head switching, and occurs when the "parallel alignment" of guide center and headwheel axis is incorrect (i.e., when the pressure of the video heads against the tape is insufficient or excessive). This form of distortion is designated "jogs" or "skew", and is shown in figure 104. Note that insufficient head-to-tape pressure causes jogs having a positive slope, while excessive head-to-tape pressure causes jogs having a negative slope. If a pulse train containing the timing discontinuities is applied to a horizontal oscillator having a "flywheel" time constant slightly greater than the 16-line head-scanning interval, a uniform pulse train of average frequency pulses is produced in which the timing variations are eliminated (figure 105). The synchroguide circuit in television receivers, and hence the horizontal deflection circuits, respond similarly. However, timing errors in blanking and picture information remain, and these errors cause the jogs mentioned above. The function of the guide servo system, then, is jog correction; and this may be accomplished manually or automatically, depending upon the operating conditions of the machine.

Another form of geometric distortion which may appear in the picture occurs when the "perpendicular alignment" of the guide center and headwheel axis is incorrect (i.e., when the head-to-tape pressure varies as a video head scans the moving tape). This form of geometric distortion is designated "scalloping", and its correction is entirely mechanical. (A third form of geometric distortion, appearing in the picture as steps, is due to slight errors in the physical placement of the video heads around the circumference of the headwheel. This distortion is known as quadrature error, and must be compensated for by manually adjusting a delay network in each of the four fm recording and playback head channels.)

Movement of the vacuum guide is controlled via mechanical linkage to the two-phase induction motor in which the reference winding is continuously excited by the power line voltage in PLAY or RECORD mode, and the control winding is driven by an error signal. Therefore, the motor shaft normally remains stationary and develops torque in one direction or the other only in response to an error signal. (The

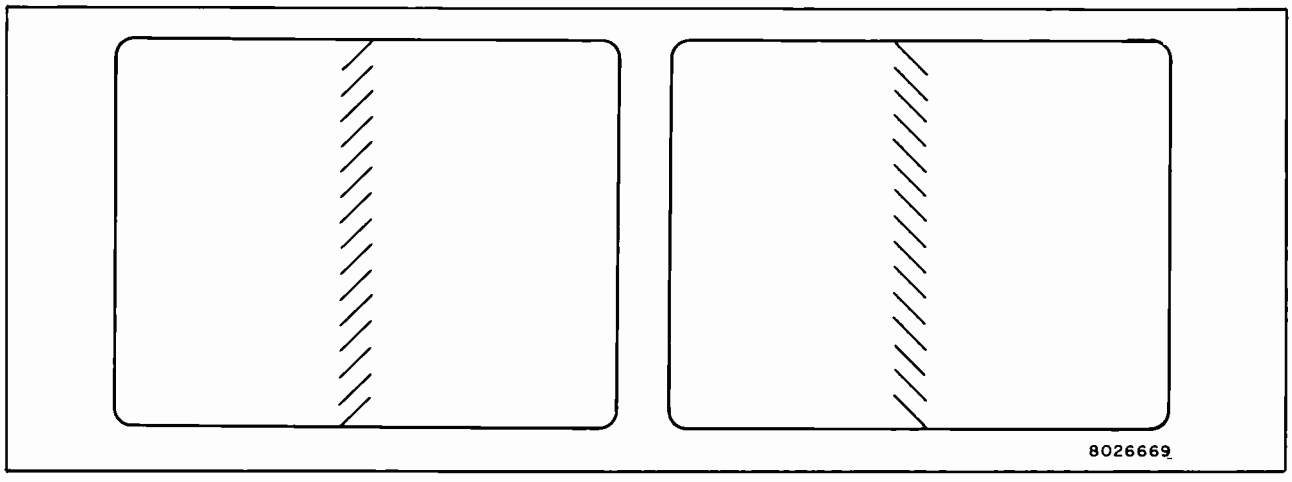


Figure 104—Sketch of TV Raster Showing Jogs Due to Insufficient Head-to-Tape Pressure (Left) and Excessive Head-to-Tape Pressure (Right)

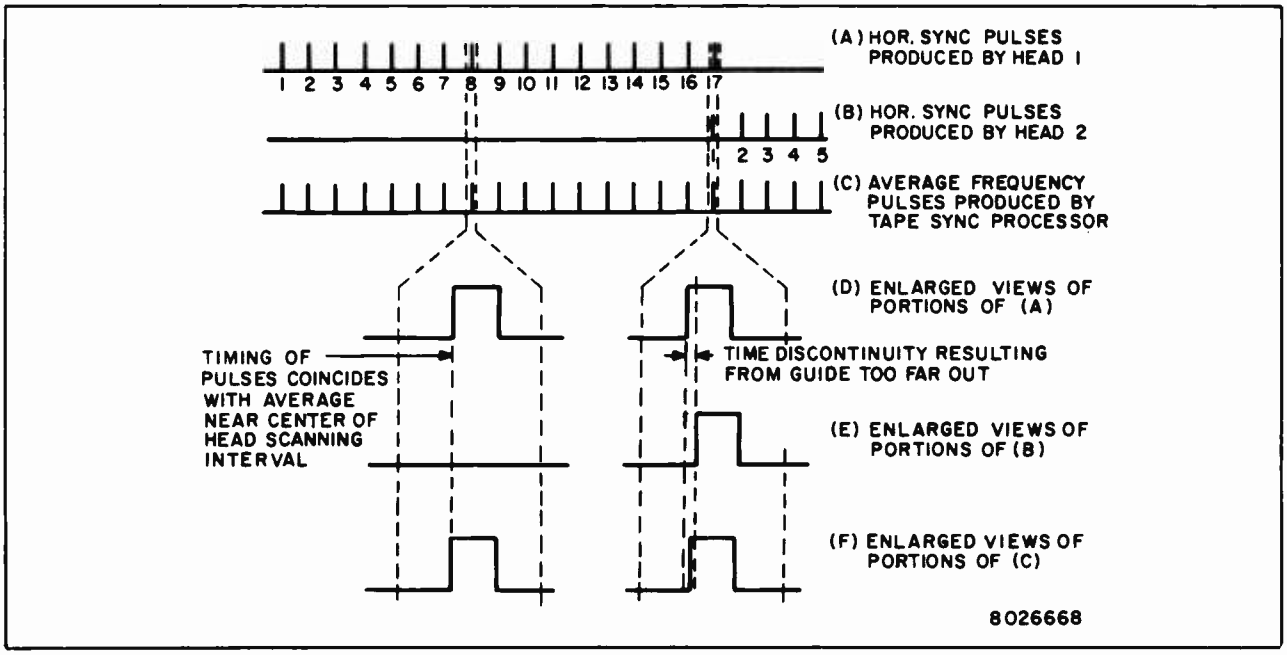


Figure 105—Waveforms Showing Timing Errors Due to Incorrect Guide Positioning During Tape Playback

direction of the torque, and thus that of the motor shaft rotation, is determined by the phase relationship between the 50/60-cycle voltages applied to the reference and control windings.) The error signal may be developed manually or automatically, depending upon the operating mode of the machine. If the guide position is controlled manually (during either tape playback or recording), the error signal is developed when a voltage unbalance exists between the center-arm of a helipot geared to the guide motor shaft and the center-arm of either the playback or record manual guide position control. If the guide position is controlled automatically (possible during tape playback only), the error signal is developed in the headwheel servo system whenever the tape horizontal sync frequency varies from the standard line frequency (15,750 cps in machines operating on 525-line standards with a 60-cycle field rate).

When guide motor torque is developed, it causes a lead screw to move in or out (depending upon the torque direction). The lead screw acts as a stop against which the guide control arm rests when the rotary guide solenoid is energized. The extension of the lead screw therefore determines the position of the vacuum guide and thus the pressure exerted on the tape by the video magnetic heads. The guide solenoid is controlled by diode matrixing circuits as shown on the *Guide Servo System Functional Diagram,* figure 127. From the diagram it may be seen that the solenoid is energized in either the PLAY or RECORD mode of machine operation, provided that the tonewheel velocity lock sense voltage is present. (The lock sense voltage is developed in the headwheel servo system when the headwheel motor has locked-in at its correct speed.) Therefore, if the machine is operated in SET-UP, STANDBY, or WIND mode, or if the headwheel motor fails to lock-in properly during tape playback or recording, the guide solenoid is deenergized and the vacuum guide is held away from the tape to prevent possible headwheel and magnetic head damage.

An additional precaution is taken to guard against headwheel and magnetic head damage when tape is being played back with the guide position controlled automatically. This precaution consists of a circuit in the demodulator output module (no. 303) which is controlled by the tape sync signal-to-noise ratio. The output of a switching transistor in this circuit is normally held at zero volts, and the guide servo is thus allowed to operate properly on automatic control. However, when the sync signal-to-noise ratio drops below a certain fixed value, —24 volts dc appears at the output of the switching transistor thus energizing the relay which places the servo in the manual control mode. Therefore, if proper head-to-tape tracking cannot be maintained, due to a failure in the capstan servo system, the tape sync will become excessively noisy and the vacuum guide will automatically revert to a preset safe manual position. This precaution is important, since an erratic error signal due to tape sync noise may cause excessive tape pressure against the headwheel.

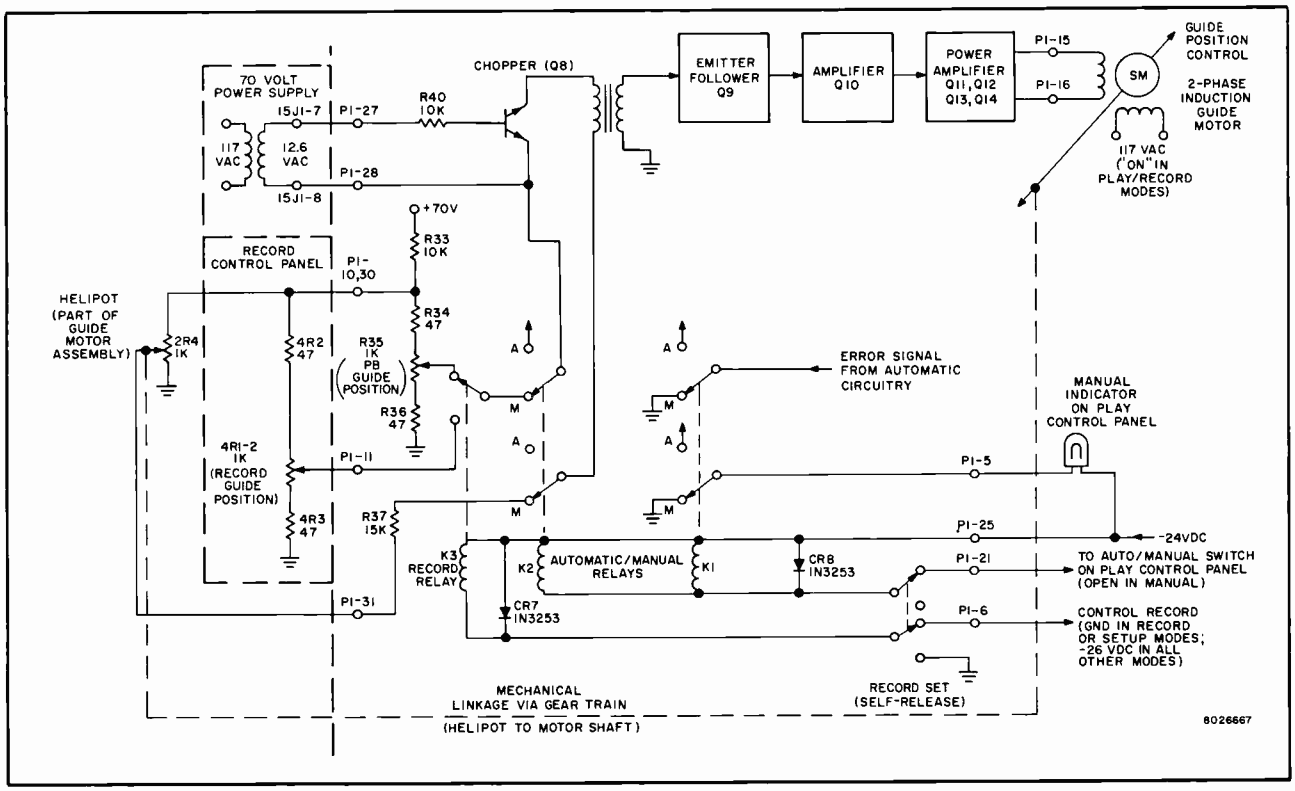


Figure 106—Guide Servo Manual Control Circuit

MODULE ANALYSIS

General

The guide servo module (no. 221) contains the circuitry required for both manual and automatic control of the vacuum guide position. (See *Guide Servo System Functional Diagram,* figure 127.) Circuits utilized in the module are controlled by relays according to the operating mode of the machine and, in PLAY mode, according to whether manual or automatic guide control is desired. In the manual mode of guide control, an error signal is developed by an unbalance in the bridge circuit consisting of a helipot geared to the guide motor shaft and either the record or playback control potentiometer, both connected across a potential of approximately 3.3 volts dc. (See block diagram, figure 106.) The d-c error signal due to bridge unbalance is converted to an a-c signal by a chopper circuit, amplified, shifted in phase by 90 degrees, and then fed to push-pull power amplifiers which produce a sinusoidal output voltage of approximately 250 volts peak-to-peak. This voltage lags or leads the voltage applied to the guide motor reference winding by 90 degrees, depending upon the polarity of the d-c error signal, and thus causes motor shaft rotation in a direction which will tend to eliminate the error. The gain of the system must be such that the bridge is always brought to a balanced condition, so that the error signal is zero. Additional gain is provided in the system to reduce drift effects which may be caused by component tolerances.

In the automatic mode of guide position control the guide position error signal is developed in the tape sync processor module (no. 317) of the headwheel servo system from the comparison of tape horizontal sync frequency with the frequency of an afc horizontal multivibrator. The 960-cycle component of the error signal is amplified, clipped, and converted into a fluctuating d-c signal by a bidirectional rectifier circuit. The resulting d-c error signal is then applied to the chopper stage where it is converted to an a-c signal and modulated, and the remaining processes performed on the error signal are identical to those described above for manual guide control. (See block diagram, figure 107.)

Two conditions must be met before automatic guide positioning may be achieved. The machine must be operated in the PLAY mode with the headwheel locked-in at its correct speed, and the tape sync must have a sufficiently high signal-to-noise ratio. Loss of headwheel lock will deenergize the guide solenoid, thereby voiding the effect of the automatic control circuitry, and a significant decrease in the tape sync signal-to-noise ratio will automatically switch the guide to a manually preset safe position.

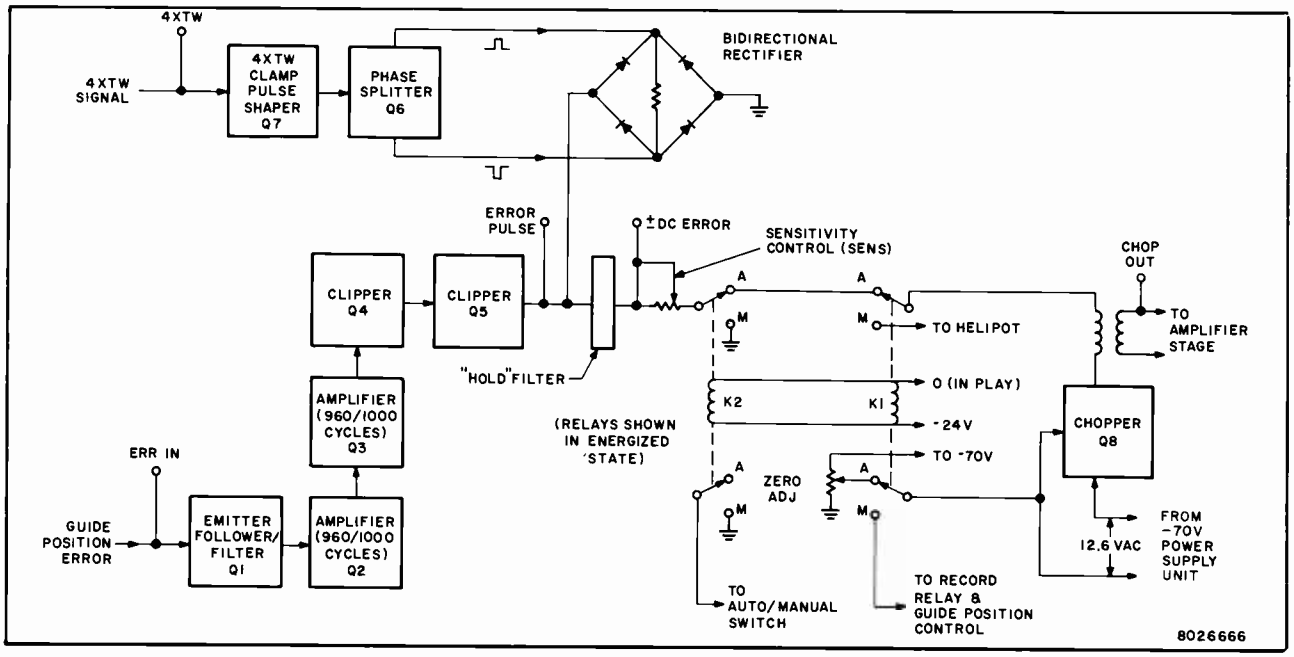


Figure 107—Automatic Guide Positioning, Block Diagram

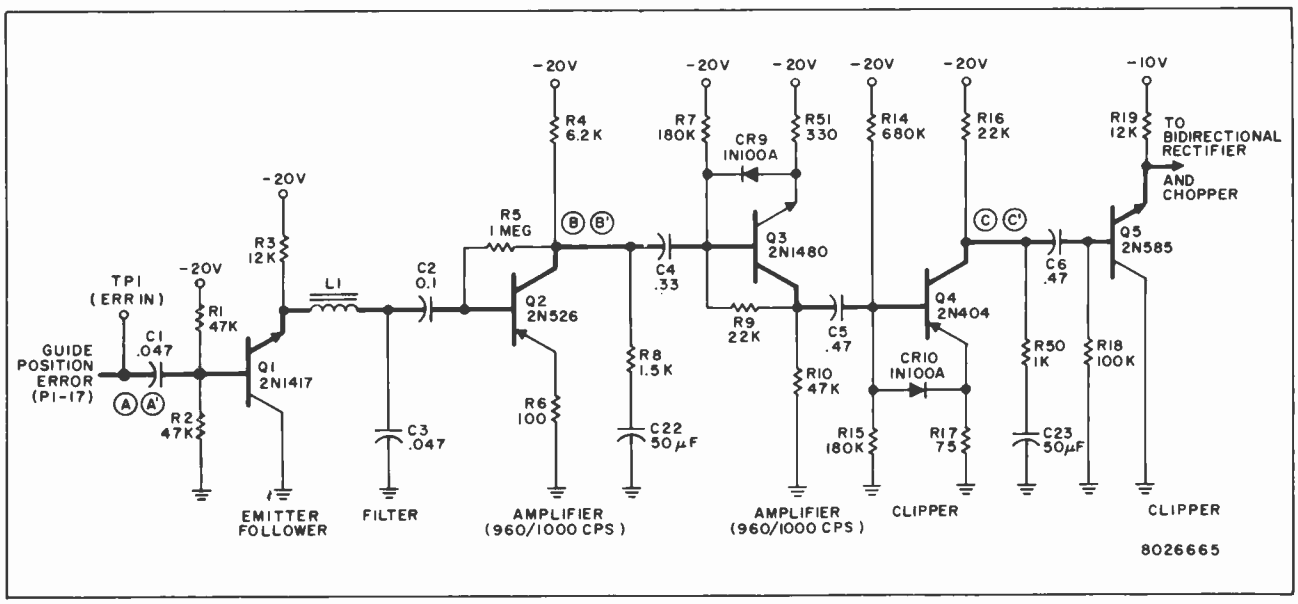
The following circuit analysis is separated into automatic and manual guide control modes. The power amplifier circuit, identical for both modes, is included with the manual control description. Waveforms and text pertain to machines operating with a 60-cycle field rate. For International machines having a 50-cycle field rate, the appropriate timing differences must be taken into consideration.

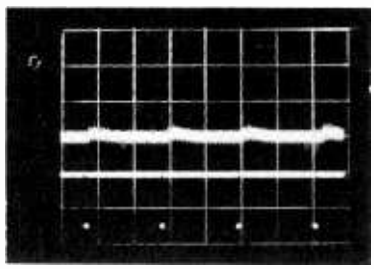
Automatic Guide Control

As shown in figure 107, the automatic guide control circuitry converts an error signal into the torque required to properly position the vacuum guide during operation in the automatic mode. The error signal utilized by the guide servo module is derived from a comparison of the horizontal afc multivibrator output (local sync) from the tape sync processor module (no. 317) with tape horizontal sync. This signal occurs at a line-frequency rate (15,750 cps in 525-line standards), and contains a 960-cycle trapezoidal error component having an amplitude which may range from .01 to .4 volts peak-to-peak. The input error signal is fed through pin 17 of plug P1 on the guide servo module to the base of emitter follower transistor Q1, and may be observed at test point TP1 (ERR IN). Figure 108A shows the error signal input at TP1 with the vacuum guide exerting insufficient pressure against the tape, while figure 108A′ shows the error signal with the guide exerting excessive pressure against the tape.

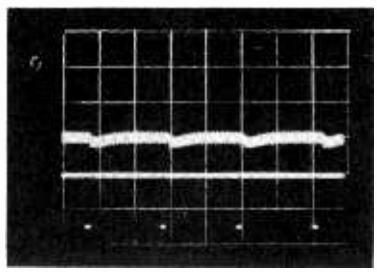
Transistor Q1, operating as an emitter follower, isolates the error generating circuits in the tape sync processor module from the low-pass filter network (coil L1 and capacitor C3) in the guide servo module. The filter network removes the line-frequency component from the error signal and converts the remaining 960-cycle trapezoidal waveform into an approximate sine wave. Transistors Q2 and Q3 in series amplify the sine wave to approximately .7 volt peak-to-peak before it is fed to clipper transistor Q4. Capacitor C22 and resistor R8 in the collector circuit of transistor Q2 provide a low-frequency bypass to ground for any low frequency transients which may appear in the input error signal. Diode CR9, in the emitter-base circuit of transistor Q3, clips the negative-going excursion of any 60-cycle transient which may appear in the 960-cycle error signal. The signals at the collectors of transistors Q2 and Q3 are shown in figure 108B with insufficient guide pressure applied to the tape, and in figure 108B′ with excessive guide pressure applied.

Following amplification by transistors Q2 and Q3, the sine wave is fed to the base of clipper transistor Q4. Transistor Q4 amplifies the sine wave and provides peak-to-peak limiting, so that the output at its collector is an approximate square wave having an amplitude ranging from 1.5 to 2 volts peak-to-peak, depending upon the magnitude of the input error signal. (Figure 108C, top, shows the signal at the collector of transistor Q4 with insufficient guide pressure applied to the tape, while figure 108C′, top, shows the signal with excessive guide pressure applied.) Diode CR10, in the emitter-base circuit of transistor Q4, clips

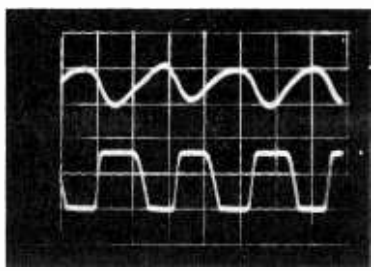




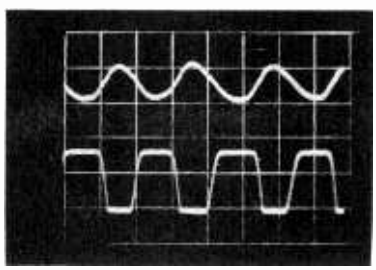
A. Top: TP1 (ERR IN), 0.5v/cm. Bottom: TP5 (4XTW), 5v/cm. Insufficient Guide Pressure



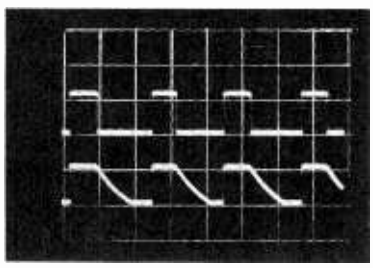
A′. Top: TP1 (ERR IN), 0.5v/cm. Bottom: TP5 (4XTW), 5v/cm. Excessive Guide Pressure



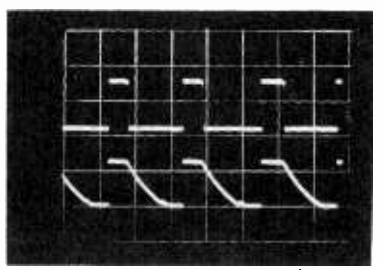
B. Top: Q2 collector, 0.5v/cm. Bottom: Q3 collector, 5v/cm. Insufficient Guide Pressure



B′. Top: Q2 collector, 0.5v/cm. Bottom: Q3 collector, 5v/cm. Excessive Guide Pressure



C. Top: Q4 collector, 2v/cm. Bottom: TP3 (ERR PUL), Q5 emitter, 2v/cm. Insufficient Guide Pressure



C′. Top: Q4 collector, 2v/cm. Bottom: TP3 (ERR PUL), Q5 emitter, 2v/cm. Excessive Guide Pressure

Machine in PLAY mode; guide in MANUAL mode with simulated errors. All sweep times 500 μsec/cm.

Figure 108—Error Signal Amplifier and Clipper Circuits

the positive-going portion of any 60-cycle transient which may appear in the 960-cycle error signal. Thus diode CR10 operates in conjunction with diode CR9 in reducing the amplitude of any 60-cycle transient which may appear in the 960-cycle error signal to a negligible value. Any low frequency transients remaining in the error signal are bypassed to ground through resistor R50 and capacitor C23 in series. It is necessary to eliminate these low-frequency transients from the error signal because if not removed they may occasionally cause the guide servo to oscillate slightly and thus produce a "hunting" effect in the picture. In isolated cases it is possible that sensitivity may go above the normal level due to wear of the mechanical system. When this occurs, "hunting" can be eliminated by reducing the servo gain with the sensitivity (SENS) control, R11.

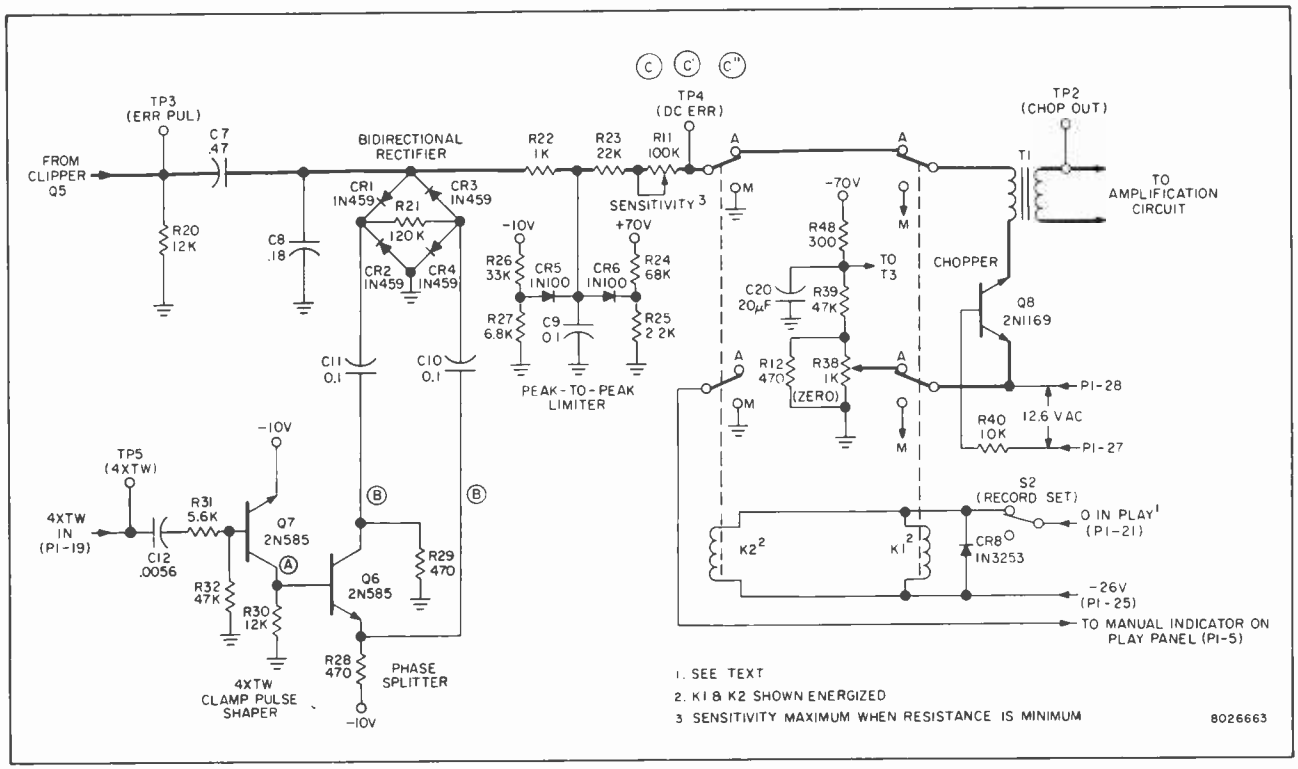
The 960-cycle square wave at the collector of transistor Q4 is fed to the base of clipper transistor Q5 which further limits the error signal. In addition to its limiting action, transistor Q5 isolates the amplification stages from the bidirectional rectifier (diodes CR1, CR2, CR3, CR4) by virtue of its operation as an emitter follower and thus its high input impedance. The output signal at the emitter of transistor Q5 is trapezoidal due to the differentiating action of resistor R20 and capacitor C7 (figures 108C and 108C′, bottom) and its polarity indicates the direction of the timing errors. This signal is used to drive the diode bridge, and may be observed at test point TP3 (ERR PUL).

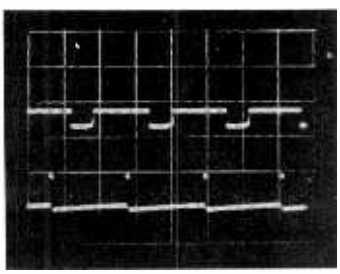
A negative-going 960-cycle pulse, locked in phase to the 240-cycle tonewheel pulse, is fed from the tonewheel processor module (no. 313) through pin 19 of plug P1 on the guide servo module to the base of transistor Q7 and may be observed at test point TP5 (4XTW). Transistor Q7 operates in a manner similar to the familiar pulse narrowing "boxcar" circuit, and produces a narrow positive-going pulse at its collector for each negative-going pulse appearing at its base (figure 109A, bottom). The positive-going pulse at the collector of transistor Q7 is fed directly to the base of phase splitter transistor Q6 which produces a positive-going pulse at its emitter and a negative-going pulse at its collector for each pulse applied to its base (figure 109B). These pulses, having amplitudes of approximately 5 volts, are then fed to opposite ends of the diode bridge where they are used in sampling the amplitude and polarity of the error signal.

The bidirectional rectifier bridge is so arranged that when a sample pulse appears it clamps the error signal to ground potential at either the positive or negative peak, depending upon the error signal polarity at the instant of sampling. This results in a fluctuating d-c output which is either positive or negative (depending upon whether the vacuum guide exerts excessive or insufficient pressure on the tape), or zero (when the guide is correctly positioned). Diodes CR5 and CR6 subject the d-c error signal to peak-to-peak limiting so that the output is limited to approximately 2 volts maximum. The design of the succeeding stages of amplification is such that maximum amplifier drive, and thus maximum torque in the guide motor, is developed at the d-c level which has been established by the limiting diodes. This design precaution insures that the various servo amplifier stages will not be overdriven by higher level error signals, and also enables the maximum velocity of correction at low error levels. (For minimum error signals the gain of the amplifiers may reach 80 db to develop full guide motor torque.) Capacitors C8 and C9 in conjunction with resistors R22 and R23 form a ladder type filter network which smooths out the d-c error signal and, in addition, potentiometer R11 (sensitivity control) and resistor R23 isolate the bridge circuit from the chopper stage which follows. Test point TP4 (DC ERR) is provided for convenience in observing the error signal output which is positive when the guide pressure on the tape is excessive (figure 109C) and negative when the guide pressure is insufficient (figure 109C′). Figure 109C″ shows the signal at TP4 with zero guide position error.

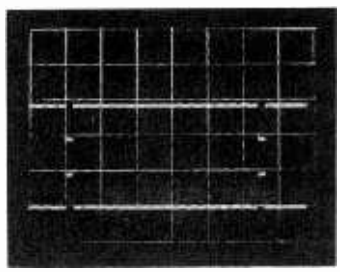
Because of the instability inherent in high gain d-c amplifiers, an a-c servo amplifier is utilized to provide drive for the control winding of the 2-phase induction motor. The chopper stage, consisting of transistor Q8, transformer T1, and associated circuit components, converts the low level d-c error signal into an a-c signal before amplification. When relay K2 is energized (guide operated in the automatic mode) the fluctuating d-c error signal is fed through the primary winding of transformer T1 to transistor Q8. Transistor Q8 is a bilateral transistor in which either electrode may act as emitter or collector. A 12.6 volt rms (35 volt peak-to-peak) 60-cycle voltage, obtained from the 70 volt d-c power supply, is applied between the base and lower emitter-collector electrode of Q8 (figures 109C′ and 109C″, bottom) and the d-c error voltage is fed to the upper electrode. The operation of the chopper stage is such that transistor Q8 conducts on alternate half-cycles of the input 60-cycle voltage, thus producing a pulsating output which is coupled through transformer T1 to emitter follower transistor Q9.

The phase and level of the pulsating output signal from transistor Q8 is determined by the polarity and level of the input d-c error voltage. A d-c path to ground is provided through potentiometer R38

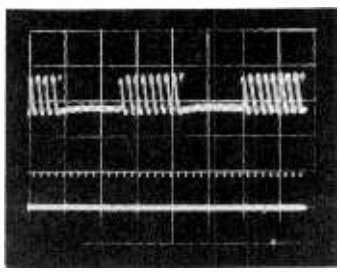




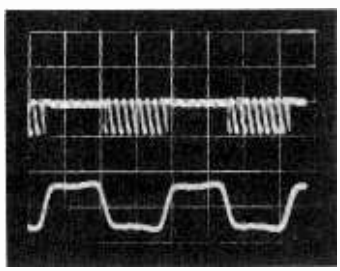
A. Top: Q4 emitter, 0.5v/cm.
Bottom: Q7 collector, 5v/cm.
(500 μsec/cm)
Insufficient Guide Pressure



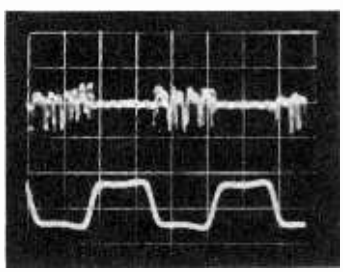
B. Top: Q6 collector, 5v/cm.
Bottom: Q6 emitter, 5v/cm.
(200 μsec/cm)



C. Top: TP4 (DC ERR), 2v/cm.
Bottom: Q6 emitter, 5v/cm.
Excessive Guide Pressure



C'. Top: TP4 (DC ERR), 2v/cm.
Bottom: Q8 base, 20v/cm.
Excessive Guide Pressure



C". Top: TP4 (DC ERR), 1v/cm.
Bottom: Q8 base, 20v/cm.
Zero Error
(Automatic Correction)

Machine in PLAY mode; guide in MANUAL mode with simulated errors. All sweep times 5 msec/cm, unless otherwise noted.

Figure 109—Bidirectional Rectifier and Chopper Circuits (Automatic Guide Control)

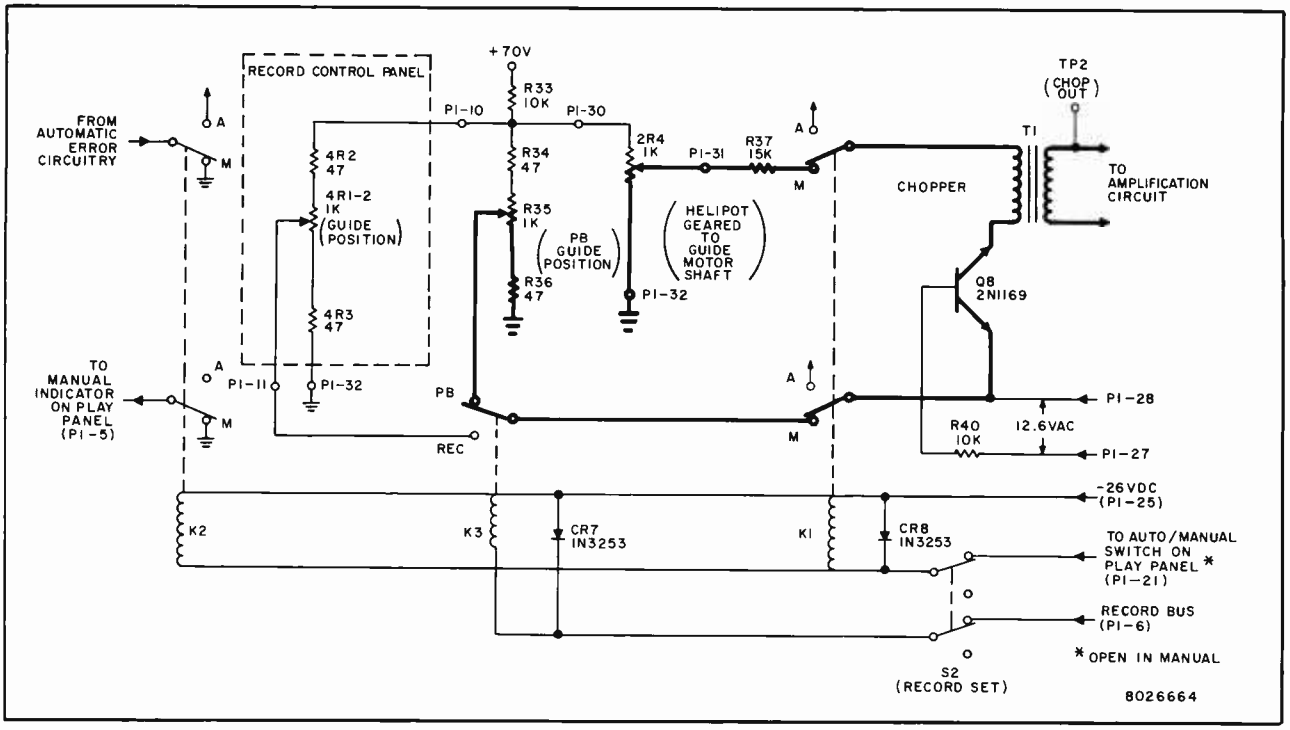


Figure 110—PLAY/RECORD Controls and Chopper Circuit (Manual Guide Control)

(ZERO), which is in series with resistors R39 and R48 to form a voltage divider network between −70 volts and ground. Potentiometer R38 is provided as an effective means of obtaining actual guide servo zero-error when operating in the automatic mode, by compensating for any unbalance which may exist in chopper transistor Q8 and in the d-c error producing circuit. In automatic operation, the error signal is developed into the requisite guide motor torque only when there is a difference between the error signal level and the potentiometer setting. Once the potentiometer has been set (see *Adjustments*) it should not require any further adjustment; however, when changing from one line-standard to another, unbalance may be introduced into the error signal circuits which will necessitate re-balancing with the potentiometer.

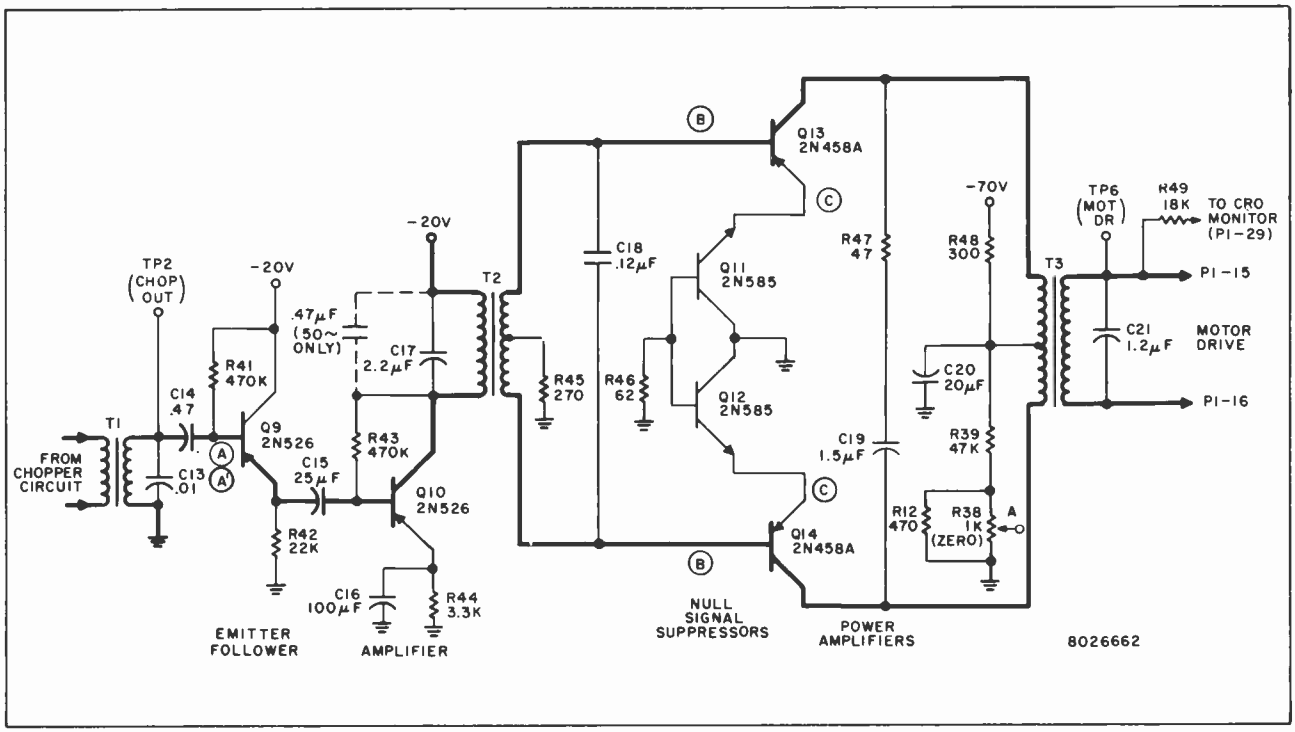
The error signal amplification stage functions during automatic guide positioning exactly as it does during manual guide positioning. Refer to figure 111 and the *Manual Guide Control* discussion for a detailed description of the amplification stage.

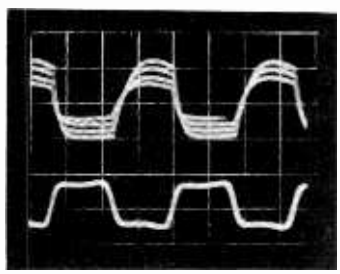
Manual Guide Control

Separate controls are provided for manually positioning the vacuum guide while either recording or playing back television tape. When recording, the guide movement is preset (as mentioned in the *Systems* discussion), utilizing the GUIDE POSITION control on the RECORD control panel. If manual operation of the guide is desired during tape playback, the PB GUIDE POSITION control on the guide servo module front panel may be utilized in manually positioning the guide after the GUIDE SERVO switch on the PLAY control panel has been pressed for MANUAL operation. However, if required, the record GUIDE POSITION control may be momentarily brought into operation (in place of the playback PB GUIDE POSITION control) by pressing the momentary-contact pushbutton on the guide servo module front panel. (See *Adjustments.*)

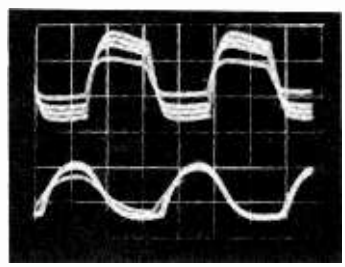
Figure 106 shows the servo loop which controls the vacuum guide movement during manual operation. In RECORD or SETUP mode, RECORD relay K3 is energized and the automatic/manual relays K1 and K2 are deenergized. This grounds the output from the automatic control circuitry and allows the voltage appearing at the center-arm of potentiometer 4R1-2 (GUIDE POSITION control located on the RECORD control panel) to be fed directly to the lower emitter-collector electrode of chopper transistor Q8 (figure 110). Simultaneously, the voltage appearing at the center-arm of potentiometer 2R4 (a helipot geared to the guide motor shaft) is fed through resistor R37 and the primary winding of transformer T1 to the upper emitter-collector electrode of transistor Q8.

In the PLAY mode, the automatic/manual relays K1 and K2 are deenergized as in the RECORD mode and the output from the automatic control circuitry

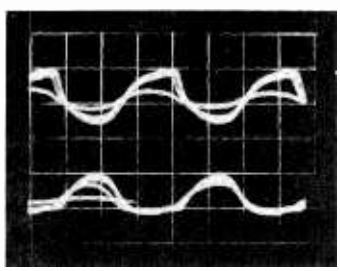




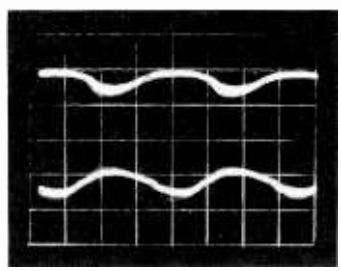
A. Top: Q9 base, 1v/cm.
Bottom: Q8 base, 20v/cm.
Insufficient Guide Pressure



A′. Top: Q9 base, 1v/cm.
Bottom: Q10 collector, 10v/cm.
Excessive Guide Pressure



B. Top: Q13 base, 2v/cm.
Bottom: Q14 base, 2v/cm.



C. Top: Q13 emitter, 2v/cm.
Bottom: Q14 emitter, 2v/cm.

Machine in PLAY mode; guide in MANUAL mode with simulated errors. All sweep times 5 msec/cm.

Figure 111—AC Servo Amplifier

is grounded; however RECORD relay K3 is also de-energized, thus allowing the voltage which appears at the center-arm of potentiometer R35 (PB GUIDE POSITION) to be fed to the lower emitter-collector electrode of transistor Q8. Also as in the RECORD mode, the voltage at the center-arm of the helipot is fed through resistor R37 and the primary winding of transformer T1 to the upper emitter-collector electrode of transistor Q8. The momentary-contact push-button switch S2 (RECORD SET) energizes RECORD relay K3 while the machine is being operated in the PLAY mode, thereby delegating control of the guide to the GUIDE POSITION control on the RECORD control panel. The purpose of switch S2 is to provide a momentary means of presetting or checking the GUIDE POSITION control for correct zero indication when the guide is properly positioned during playback of a test tape or other suitable tape (see *Adjustments*). If the switch is pressed during machine operation in PLAY (automatic guide control), RECORD, or SETUP modes, it will have no effect on the guide control circuits.

When either guide position control is adjusted (depending upon the operating mode of the machine), a difference in potential is established between the emitter-collector electrodes of chopper transistor Q8. This potential difference constitutes the d-c error voltage, which must be amplified before it can be utilized in effectively controlling the vacuum guide motor.

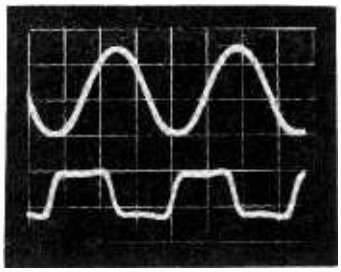
Transistor Q8 is a bilateral transistor (i.e., either electrode may function as emitter or collector) with a 12.6 volt rms (35 volt peak-to-peak) 60-cycle voltage, obtained from the 70-volt power supply, applied between its base and lower emitter-collector electrode. (Note that in International machines a 50-cycle voltage is applied to the chopper transistor.) The operation of the chopper stage is such that transistor Q8 conducts on alternate half-cycles of the input 60-cycle voltage, thus producing a pulsating output. As the d-c voltage on the lower emitter-collector electrode of transistor Q8 is varied (by adjusting either of the guide position controls, depending upon the operating mode of the machine), an unbalanced condition is developed in the chopper circuit which results in the generation of the vacuum guide error signal. The phase of the error signal is determined by the polarity of the d-c voltage applied to transistor Q8 from either guide position potentiometer with respect to the voltage applied to the transistor from the helipot geared to the guide motor shaft; i.e., as the polarity of the d-c signal reverses, the phase of the a-c output signal shifts 180 degrees. The amplitude of the output signal is then proportional to the difference in magnitude of the d-c voltages applied to the chopper transistor.

Transformer T1 couples the pulsating error signal from transistor Q8 to the base of emitter follower transistor Q9, and provides signal gain at a ratio of approximately 1 to 3. The amplified error signal may be observed at test point TP2 (CHOP OUT). Figure 111A shows the error signal at the base of transistor Q9 which will result in a correction to increase vacuum guide pressure, while figure 111A′ shows the error signal which will introduce a correction to decrease the guide pressure. Emitter follower transistor Q9 isolates the chopper circuitry from the amplification stages which follow, and the signal at the emitter of Q9 is fed to amplifier transistor Q10 which drives transformer T2 in addition to providing a small amount of signal gain. Transformer T2 is tuned for 60-cycle operation by capacitors C17 and C18 which are connected across the transformer primary and secondary windings respectively. (For 50-cycle International operation, a .47 μfd capacitor is connected in parallel with C17.)

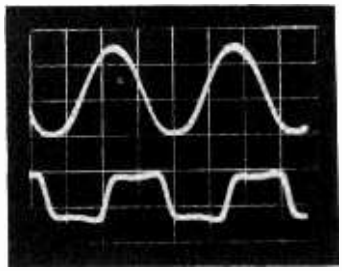
The output from transformer T2 is a sinusoidal signal having an amplitude of approximately three volts peak-to-peak. This signal is fed to the bases of power amplifier transistors Q13 and Q14 from opposite ends of the transformer, and thus the transistors are driven by signals which are 180 degrees out of phase, (figure 111B). Transistors Q13 and Q14, and associated circuit components, form a class AB push-pull amplifier stage which provides a 250-volt peak-to-peak sinusoidal power output to the 5500 ohm load of the guide motor control winding via the impedance matching output transformer T3.

Transistors Q11 and Q12, in the power transistor emitter return paths, are null-signal suppressors and their purpose is to clip the a-c signal developed by transients in the chopper stage at zero error (null balance). The transistors are effective in attenuating a 20 volt peak-to-peak null signal to approximately 2 volts peak-to-peak during normal operation, thus keeping the vacuum guide stationary and eliminating the possibility of jitter around the zero setting of the guide.

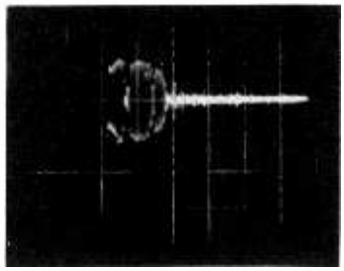
Tuning capacitors C19 and C17, in the power amplifier circuit, shift the phase of the sinusoidal error signal so that the output voltage fed to the vacuum guide motor control winding either lags or leads the sinusoidal voltage applied to the motor reference winding by the required 90 degrees. (A .47 microfarad capacitor is connected in parallel with C17 to obtain the 90-degree phase shift when the machine is operated on 50-cycle power.) The direction of guide motor shaft rotation depends upon whether the control voltage lags or leads the reference voltage, and this is in turn determined by the polarity of the d-c error signal fed to the chopper circuit.



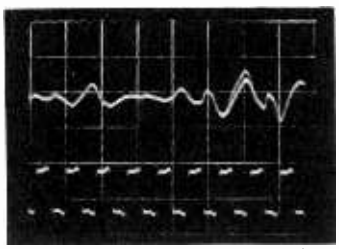
A. Top: TP6 (MOT DR), 100v/cm.
Bottom: Q8 base, 20v/cm.
(5 msec/cm)
Insufficient Guide Pressure



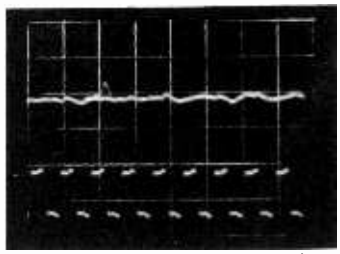
B. Top: TP6 (MOT DR), 100v/cm.
Bottom: Q8 base, 20v/cm.
(5 msec/cm)
Excessive Guide Pressure



C. TP6 (MOT DR), 100v/cm.
(200 msec/cm)
Automatic Correction for
Manual Error Insertion



D. Top: TP6 (MOT DR), 2v/cm.
Bottom: Q8 base, 20v/cm.
(20 msec/cm)
Zero Error
(Automatic Correction)



E. Top: TP6 (MOT DR), 2v/cm.
Bottom: Q8 base, 20v/cm.
(20 msec/cm)
Manual Zero

Machine in PLAY mode; guide in MANUAL mode with simulated errors.

Figure 112—Waveforms Obtained at Test Point TP6 (MOT DR)

Figure 112 shows the motor drive waveforms obtained at test point TP6 (MOT DR) during various modes of guide motor control. A and B of figure 112 illustrate the 90-degree phase shift between the 250-volt peak-to-peak control voltage waveform and the voltage waveform applied to the chopper stage, which is derived from the same source as is the reference voltage. In figure 112A the control voltage lags the reference voltage by 90 degrees, and thus causes the guide motor shaft to rotate in a direction which tends to increase guide pressure against the tape. In figure 112B the control voltage leads the reference voltage by 90 degrees, and the motor shaft rotates in the opposite direction to decrease guide pressure. Figure 112C shows the waveform obtained when a guide position error of approximately 1/3 inch is manually introduced and then automatically corrected. (Deliberate manual insertion of a guide position error is part of the procedure for checking the automatic zero adjustment, as explained in the *Adjustment* section.) Figures 112D and 112E show the zero error signals obtained at TP6 while operating the guide automatically and manually respectively.

The motor drive signal is also fed to the CRO monitor switcher, and may be observed on the CRO monitor when the GUIDE SERVO pushbutton switch on the monitor switcher is depressed. This provides a means of rapidly checking the servo control output, so that the operation of the guide servo may be examined during manual or automatic control, as the error correction takes place from maximum output to null. (Refer to waveforms in figure 112.)

SETUP ADJUSTMENTS

The following setup adjustment procedures are not routine, but should be performed whenever the operation of the vacuum guide indicates that they are necessary. Equipment required while making the adjustments includes an RCA alignment test tape (MI-40793) and a 1/4-inch open-end wrench (MI-40742, item 7).

Before proceeding with the adjustments below, make the vacuum guide position, scallop, and head quadrature adjustments as outlined on page 15 and 19 of the *TR-22 Operation Manual* (IB-31197).

Jog Adjustment

1. Play back the alignment test tape, press the GUIDE SERVO selector switch for MANUAL guide position control, and set the PB GUIDE POSITION control on the guide servo module front panel to "0" on the scale. (Check to make certain that the GUIDE POSITION control on the RECORD control panel is locked in the "0" position. If necessary unlock the control, set it to "0", and re-lock it.)

2. Hold down the momentary-contact RECORD SET button on the guide servo module front panel and, using the 1/4-inch open-end wrench, turn the hex head penetration range adjustment screw (figure 113) until all jogs are eliminated. If the picture on the monitor appears as shown in figure 114, turn adjustment screw in to increase penetration and eliminate jogs. If the picture appears as shown in figure 115, turn adjustment screw out to decrease penetration and eliminate jogs.

3. To insure an accurate setting, open and close the vacuum guide several times by first pressing the PLAY pushbutton and then, after the vacuum guide closes, pressing the STOP pushbutton.

4. The picture should now appear as shown in figure 116.

> NOTE: If steps are present in the picture pattern, a re-adjustment of the head quadrature is required. Follow the procedure outlined on page 19 of the *Operation Manual* (IB-31197) to make this adjustment.

Zero Adjustment

1. Play back the alignment test tape, or picture information containing vertical bars.

2. Press the GUIDE SERVO selector switch for MANUAL guide position control and rotate the PB GUIDE POSITION control on the guide servo module front panel to obtain straight vertical bars.

> NOTE: Start with minimum pressure setting and rotate the PB GUIDE POSITION control in a clockwise direction only, to obtain the straight vertical bars (i.e., without any to-and-fro movement around the correct setting). This precaution will eliminate possible error due to mechanical back-lash when the machine is re-started with manual guide control.

3. Press DEMOD OUT pushbutton on picture monitor switcher and observe picture on monitor to ascertain that the four individual channel and combined video equalization adjustments have been properly made to obtain the best possible picture with minimum noise.

4. Make the quadrature error and scallop adjustments if necessary to obtain perfectly straight vertical bars.

5. Press the GUIDE SERVO selector switch to obtain automatic (AUTO) guide positioning.

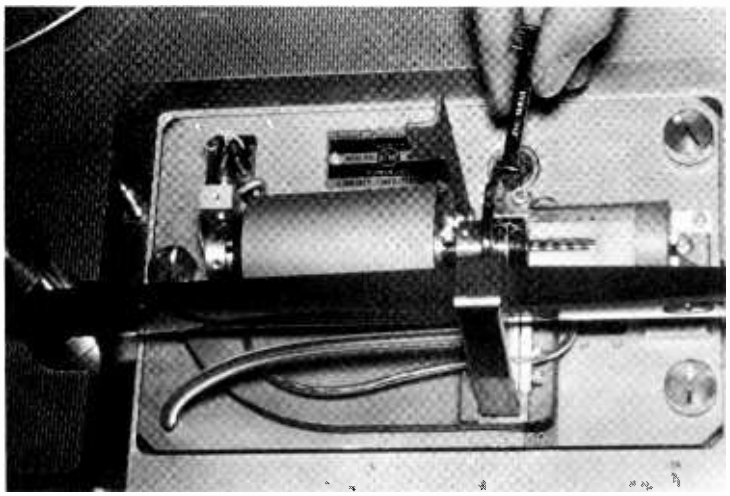


Figure 113—Guide Servo Mechanical Adjustment

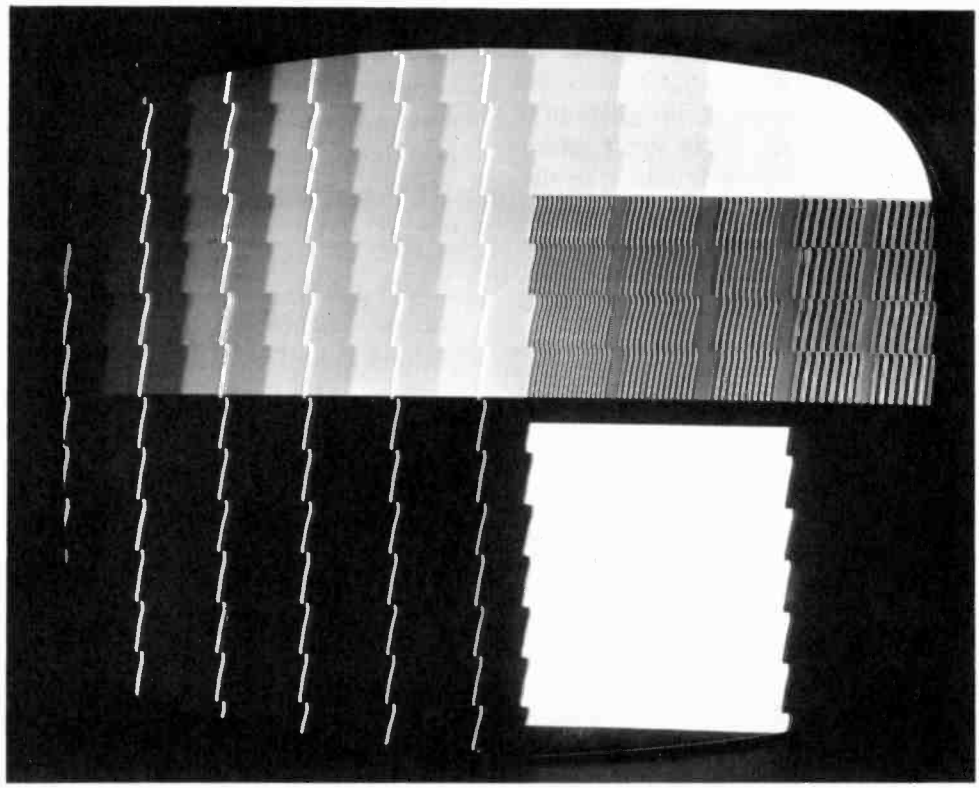


Figure 114—Jogs in Bar Pattern (Insufficient Head Penetration)

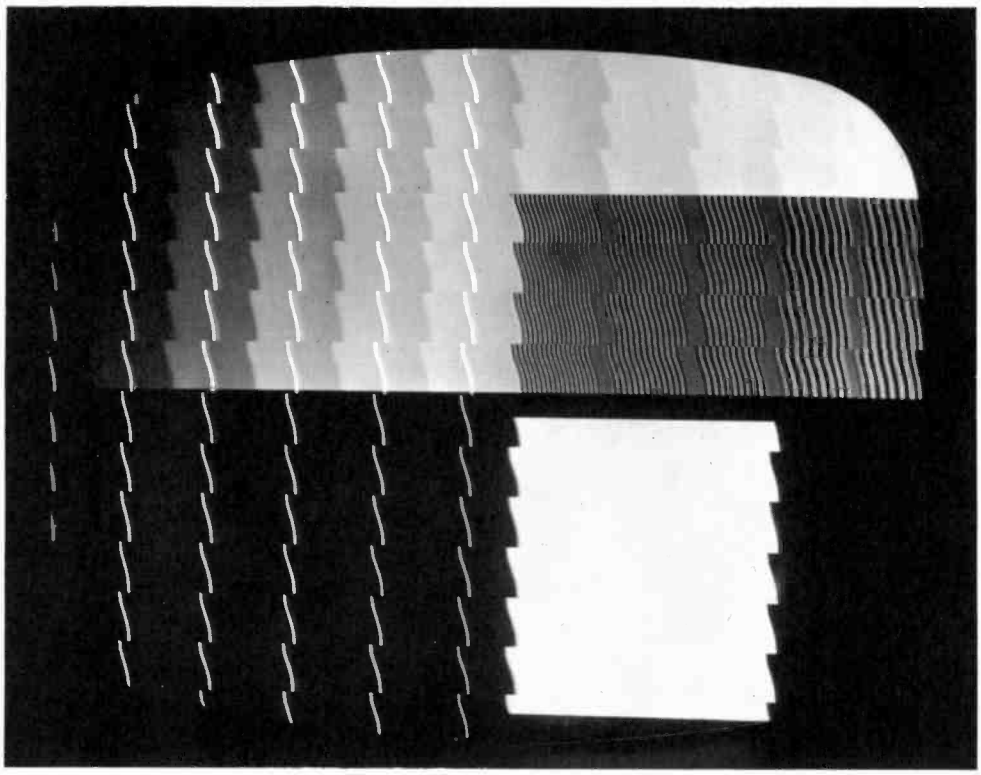


Figure 115—Jogs in Bar Pattern (Excessive Head Penetration)

6. Make certain that the sensitivity (SENS) control on the guide servo module front panel is rotated to its maximum clockwise position; then introduce an error by applying a slight pressure to the guide in a direction toward the headwheel. If the guide settles down to the point where no error is visible in the vertical bars of the picture observed on the monitor, the ZERO screwdriver adjustment on the guide servo module front panel is correctly set. If an error remains in the vertical bars of the picture, the ZERO adjustment must be reset as described in steps 7 and 8.

NOTE: If "hunting" or a slight to-and-fro displacement of head transitions is observed in the vertical bars, first operate the guide manually to make certain the vertical bars played back from the alignment tape are actually stationary, then operate the guide automatically once again with the sensitivity control rotated counter-clockwise just enough to keep the vertical bars stationary in the automatic mode.

7. If the guide leaves a slight error toward the right of the picture, reset the ZERO adjustment very slightly in the clockwise direction. Apply a slight pressure to the guide once again, and observe the error in the picture. Repeat this process, resetting the ZERO adjustment in minute increments each time, until the error has been eliminated.

8. When the ZERO adjustment has been correctly set, start the machine on automatic (AUTO) guide position control with simulated errors (introduced by the manual PB GUIDE POSITION control) in either direction, and ascertain that after automatic correction, no guide error is present.

9. Re-set the PB GUIDE POSITION control to its correct position, as described in step 2. (Refer to figure 112C.)

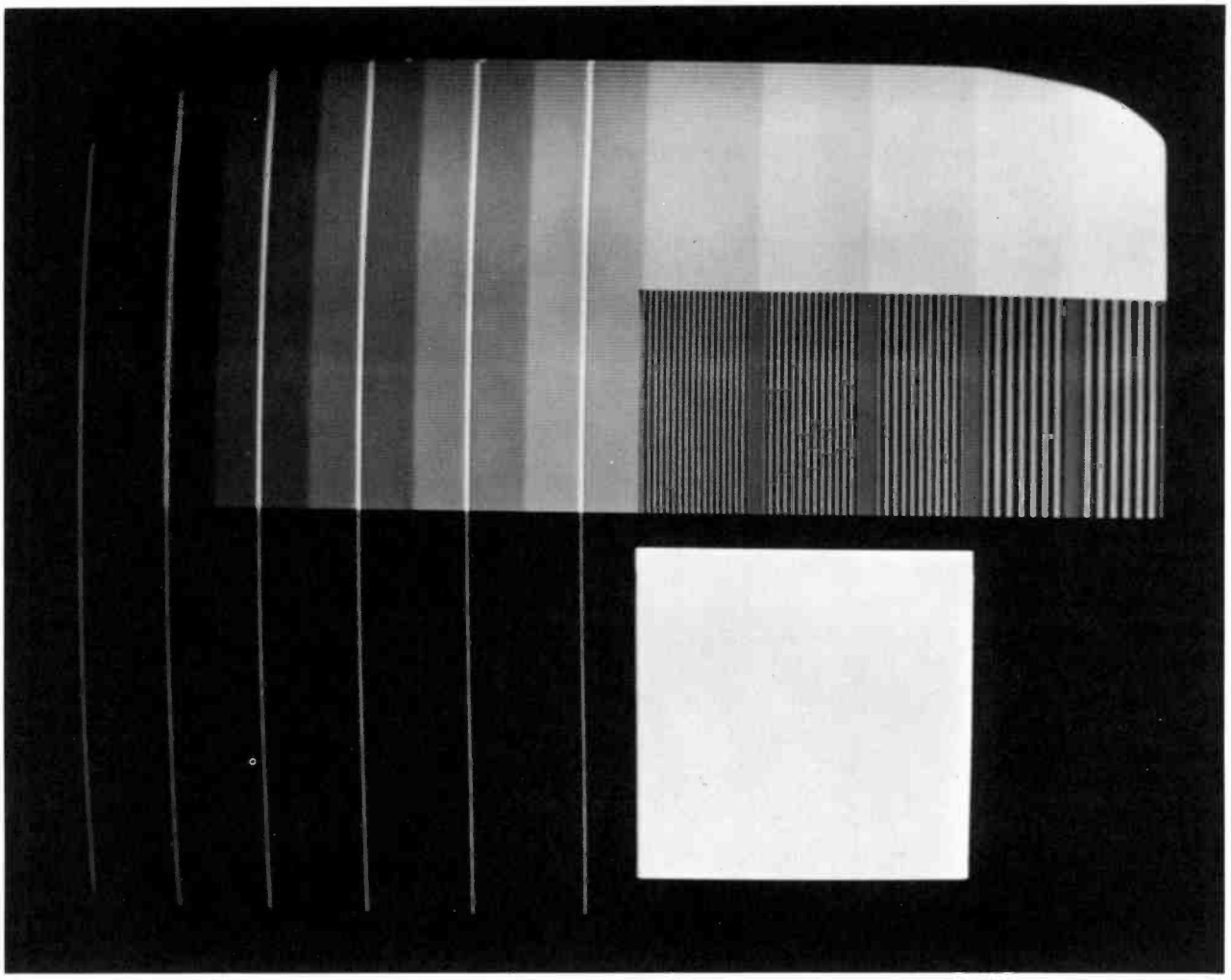


Figure 116—Normal Appearance of Alignment Tape Playback

TROUBLE-SHOOTING CHART

Fault	*Possible Cause*	*Remedy*
"Hunting"	Sensitivity too high.	Turn sensitivity control (SENS) on guide servo module front panel counter-clockwise just enough to prevent hunting. If hunting persists with the sensitivity control fully counter-clockwise, see step below.
	Split nut on guide mechanism too loose.	(a) Remove headwheel panel and tighten split nut so that it is snug; i.e., neither too loose nor too tight. IMPORTANT: The vacuum guide lead screw should be lubricated monthly, utilizing the lubricating grease provided in the MI-40742 Accessory Kit (item 18). (b) After tightening the split nut, adjust ZERO setting as described in the *Setup Adjustments* section (step 6). Make certain that the guide rapidly returns to a "null" when a minute error is introduced in either direction by applying a slight pressure to the guide in a direction toward the headwheel as the tape is played back for a picture without quadrature errors.
"Zero-drift" (The guide movement is apparently sluggish)	Once correctly set, the ZERO adjustment should remain fixed. However, if an error remains in either direction, the guide servo system is not responding rapidly enough to minute errors.	(a) Turn sensitivity control (SENS) on guide servo module front panel clockwise to eliminate the minute error. (b) If an error remains, observe the waveform on the CRO monitor with the GUIDE SERVO pushbutton on the CRO monitor switcher depressed. The waveform should indicate low frequency excursions having amplitudes of approximately 30 to 50 volts peak-to-peak, as compared with servo operation with a 250 volt peak-to-peak signal. If the waveform is steady, as it is during the manual "null", check waveforms in the automatic guide control circuitry to trace the fault. (c) If guide does not respond to 30 to 50 volt peak-to-peak excursions during automatic operation, check split nut on guide servo mechanism to ascertain that it is not too tight.
Guide fails to "lock-in" automatically.	Trouble in tape sync switching circuit of demodulator output module (no. 303).	(a) Check for zero voltage reading at pin 21 of plug P1 on guide servo module. (b) If voltage reading is approximately —24 volts dc, check sensitivity of the switching circuit in the demodulator output module. (The guide changeover from automatic to manual operation must occur only during conditions of an exceptionally noisy picture.)
Guide does not "pull-in" from one direction only.	Defective phase splitter transistor Q6 (type 2N585).	Check 5 volt positive and negative clamp pulses. Replace transistor Q6 if pulses are not equal in magnitude.
Guide shaft binds at one end.	Guide mechanism may have exceeded normal position-setting range.	(a) Remove headwheel panel, operate the machine in WIND mode with no tape movement, and observe that the shaft rotates when the manual guide position control is varied from one extreme position to the other. (If the output 250 volt peak-to-peak signal does not null at any setting of the guide position control, the manual loop is open.) (b) If the shaft still binds at the lower end, a helipot adjustment is required. This adjustment is made as described on page 23 of the *TR-22 Television Tape Recorder, Tape Transport* instruction book (IB-31648), utilizing the vacuum guide alignment jig (MI-40665).

POWER AMPLIFIERS

MODULE CIRCUIT DESCRIPTION

General

Five power amplifiers (module nos. 330 through 334) furnish the power required to drive both the headwheel motor and the capstan motor. The capstan motor is a two-phase synchronous type which requires two 60-cycle voltages differing in phase by 90 degrees. These voltages are developed in the capstan oscillator module (no. 322) and each is fed to a separate power amplifier (module nos. 330 and 331). The headwheel motor, which is a three-phase synchronous type, requires three power amplifiers (module nos. 332, 333, and 334) to provide the power gain necessary to drive the motor. The input voltages to the headwheel power amplifiers are 480-cycle voltages, differing in phase by 120 degrees, and are obtained from the headwheel modulator module (no. 315). Since the circuitry of each of the five power amplifier modules is identical to that of the others, the modules are interchangeable.

In each module, to insure positive contact between certain pins of plug P1 and corresponding pins of the plug receptacle, jumpers are connected between the pins through which the input, output, and operating voltages are fed and blank pins on the plug and receptacle. (E.g., the input a-c voltage to each module is fed simultaneously from pins 19 and 9 of the receptacle to pins 19 and 9 of the module plug.) Each module contains a double interlock. When the module plug is not securely inserted into its receptacle, one of the interlocks (between pins 8 and 24) will cause the MODULE lamp (above the left-hand side of the tape transport panel) to be illuminated. At the same time, the second interlock (between pins 10 and 26) causes the machine to enter and remain in the STOP mode. Figure 117 is a block diagram of a power amplifier module.

Filter-Regulator

The filter-regulator circuit consists of transistors Q1, Q2 and associated circuit components (figure 118). The primary purpose of this circuit is to provide a degree of isolation which will suppress any crosstalk occurring between the headwheel and capstan power amplifiers through the −70 volt input to the modules. (An additional function of the filter circuit is to filter out most of the ripple voltage which may be present in the −70 volt line.)

The negative 70 volts dc, obtained from the 70 volt power supply via terminal block 11TB1-1, is fed to the module through pin 5 (jumpered to pin 27) of plug P1. From pin 5, the negative voltage is fed through fuse F1 (3 amperes), which is in parallel with a lamp, to the regulator circuit. When a component failure within the power amplifier module causes a current drain exceeding 3 amperes, the fuse opens and the lamp (located on the module front panel) is illuminated. Thus the filter-regulator circuit is protected from excessive current drain due to a failure elsewhere in the power amplifier module.

Transistors Q1 and Q2 are effectively operated as emitter followers in cascade, and their beta product multiplies the 20 μfd capacitance of capacitor C1 to obtain a very large output capacitance, and thus a very low capacitive reactance at low frequencies for efficient filtering action. Resistors R3 and R4 form a voltage divider network which places approximately −68 volts dc on the base of transistor Q1. This voltage drives transistor Q1 into conduction and the potential at its emitter, and thus at the base of transistor Q2, is also approximately −68 volts.

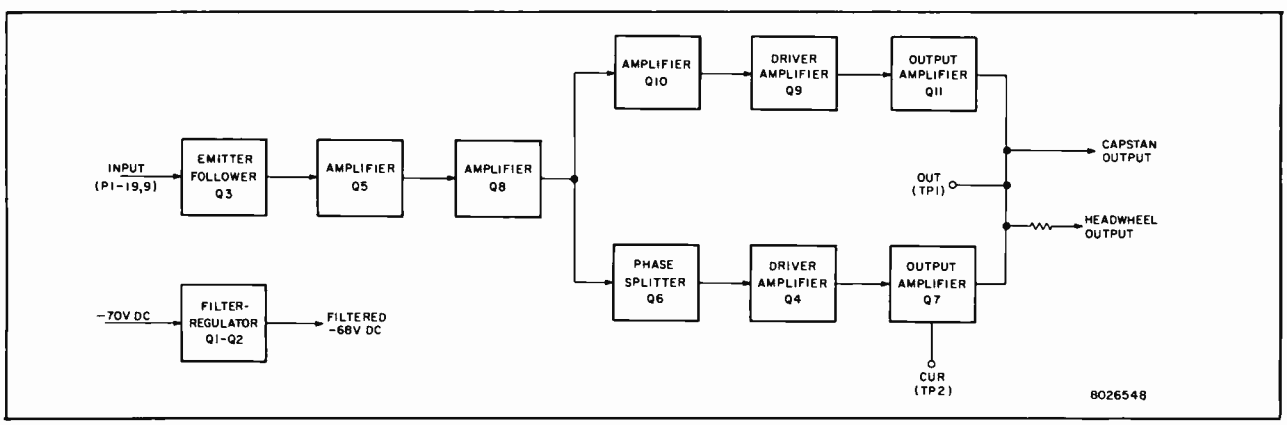


Figure 117—Power Amplifier Module Block Diagram

Amplifier Circuits

The sinusoidal input voltage fed to the power amplifier module through pin 19 (jumpered to pin 9) of plug P1, occurring at a 60-cycle rate in the capstan servo system and at a 480-cycle rate in the headwheel servo system, is coupled by capacitor C2 to the base of transistor Q3 (figure 119). Transistor Q3 functions as an emitter follower, and its purpose is to isolate the input from the succeeding amplification circuits while at the same time maintaining a relatively constant input impedance. The negative bias potential applied to the base of transistor Q3 from the voltage divider network consisting of resistors R14, R10, and R11 is nominally −6.7 volts, and the d-c potential applied to the emitter of Q3 is maintained at a constant level of approximately −6.6 volts by the voltage divider network consisting of resistors R14, R16, and R13. Transistor Q3 is thus forward biased and will pass the normal a-c signal fed to its base. However, when the input signal amplitude becomes excessive, as it may when the headwheel motor is starting up, the transistor is driven alternately into saturation and cut-off and thus a protective limiting action occurs.

The signal at the emitter of transistor Q3 is fed directly to the base of amplifier transistor Q5, which is biased into conduction by the constant negative d-c potential developed across resistor R13. The primary function of transistor Q5 is to complete an a-c negative feedback loop whose purpose is to provide gain stabilization. In the feedback loop, the output current at the collector of output amplifier transistor Q7 is fed back to the emitter of transistor Q5 and is 180 degrees out of phase with the current flowing in the base circuit of Q5. Thus, due to the phase shift at the emitter of transistor Q5 the feedback is degenerative and stabilization is achieved. In the power amplifier modules, transistor Q5 and resistor R17 in series form a path through which the required current is drawn from the +10 volt dc supply.

The sinusoidal signal appearing at the collector of transistor Q5 is fed directly to the base of amplifier transistor Q8. The amplitude of this signal is low (approximately 1.5 volts peak-to-peak) due to the negative feedback in the emitter circuit of transistor Q5. When transistor Q5 conducts, the d-c potential at its collector is approximately −0.9 volt. Since this potential also appears on the base of transistor Q8, the transistor is biased into conduction. Because of a high load impedance in the collector circuit of transistor Q8, the voltage gain of the stage is very high. Frequency roll-off is accomplished by capacitor C4, in the base circuit of transistor Q8, which by-passes any high frequency signal components to ground.

The voltage amplified sinusoidal signal at the collector of transistor Q8 is fed simultaneously to parallel current amplification chains consisting of transistors Q10, Q9, Q11 and Q6, Q4, Q7. Bias potentials applied to transistors Q6 and Q10 are such that Q6, an NPN type, conducts only during the positive portion of the sinusoidal signal fed to its base, while Q10, a PNP type, conducts only during the negative portion of the signal fed to its base. Therefore a phase-splitting action occurs and each half-cycle of the sinusoidal output from transistor Q8 is passed through a separate current amplification chain.

Transistors Q6, Q4, and Q7 form the chain which provides the current gain for the positive half-cycle of the sinusoidal signal. The d-c potentials at the base

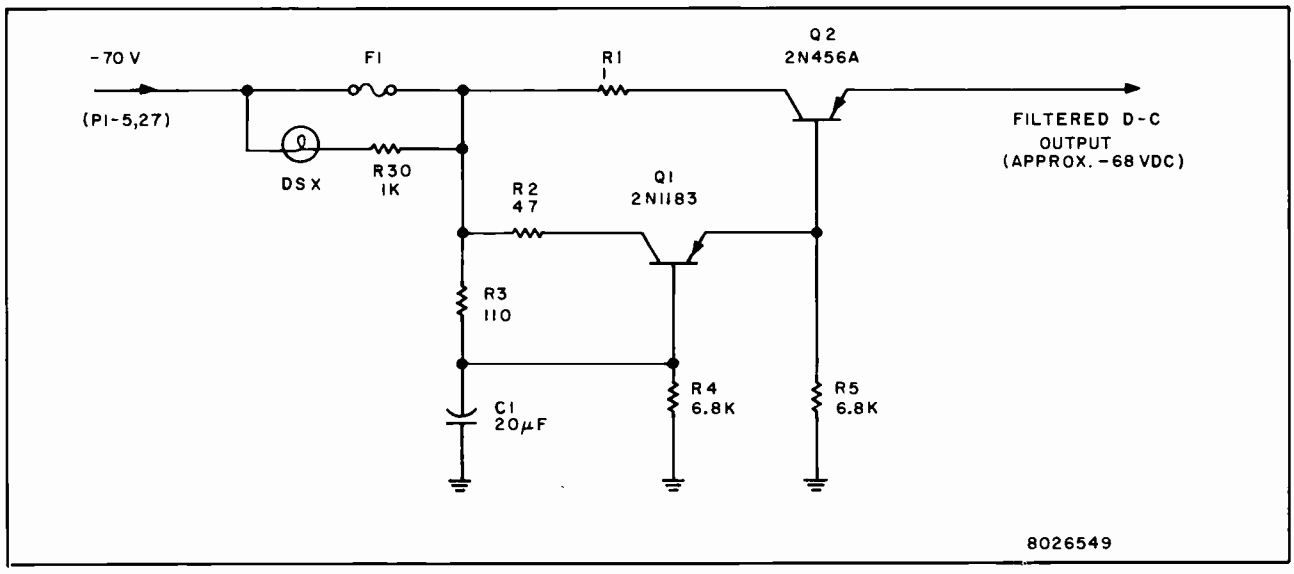


Figure 118—Filter-Regulator Circuit

and emitter of transistor Q6 are such that with no input signal the transistor is cut off. However during the positive half-cycle of the sinusoidal signal fed to the base of transistor Q6 the transistor conducts, and a negative-going pulse appears at its collector. The negative-going pulse is fed directly to the base of driver amplifier transistor Q4 and causes Q4, normally cut-off, to conduct. When transistor Q4 conducts, a negative-going pulse appears at its emitter and is fed directly to the base of output amplifier transistor Q7. Transistor Q7 is normally biased into cut-off by the d-c potential applied to its base from the +10 volt supply. When the negative-going pulse is fed to the base of transistor Q7, the transistor conducts and a positive-going pulse appears at its collector.

The negative half-cycle of the sinusoidal output from amplifier transistor Q8 is passed through the current amplification chain consisting of transistors Q10, Q9, and Q11. These transistors are PNP types, and function as emitter followers which conduct only when negative-going pulses are applied to their bases. Thus the negative half-cycle of the sinusoidal waveform fed to the base of transistor Q10 causes the transistor to conduct, and a negative-going pulse appears at its emitter. Since transistors Q10, Q9, and Q11 function as emitter followers, the output pulse at the emitter of output amplifier transistor Q11 will also be a negative pulse. This pulse is then combined with the positive-going output pulse at the collector of output amplifier transistor Q7. Because the pulses are 180 degrees out of phase, due to the phase-splitting action of transistors Q6 and Q10 as mentioned above, they combine to form the motor drive sine wave. In this manner the current amplifier chains provide the current gain required to drive either the capstan or the headwheel motor.

To maintain a proper balance between the positive- and negative-going pulses which combine to form the output sinusoidal signal, the d-c potential on the collectors of transistors Q4 and Q7, and on the emitter of transistor Q6, must be approximately one-half that on the collectors of transistors Q10, Q9, and Q11. This potential is maintained at a constant level (nominally −32 volts dc) by d-c feedback which is actually the instantaneous value of the a-c feedback mentioned above in conjunction with gain stabilization.

The fluctuating d-c current flowing in the emitter circuit of output amplifier transistor Q7 may be measured by observing the voltage waveform at test point TP2 (CUR) and dividing the voltage amplitude by the emitter resistance (0.5 ohm). Test point TP1 (OUT) is provided for convenience in observing the power amplifier output voltage. In the capstan amplifier modules (nos. 330 and 331), the output voltage is fed directly to pins 18 and 22 of plug P1. However, in the headwheel power amplifier modules (nos. 332, 333, and 334), the output voltage is fed through resistor R29 to pins 17 and 6 of plug P1. Resistor R29 (1 ohm) is provided for isolation purposes; i.e., to eliminate cross-talk between the phases of the 3-phase motor drive sine wave.

The 60-cycle output voltages from the capstan power amplifier modules differ in phase by 90 degrees and have an amplitude of approximately 17 volts rms. The voltages are fed from pin 18 of plug P1 through electrolytic capacitors 11C1 and 11C2 (located on the rear shelf) to transformers 11T1 and 11T2 (figure 120). Capacitors 11C1 and 11C2 block the d-c component of the output voltage and have high capacitance

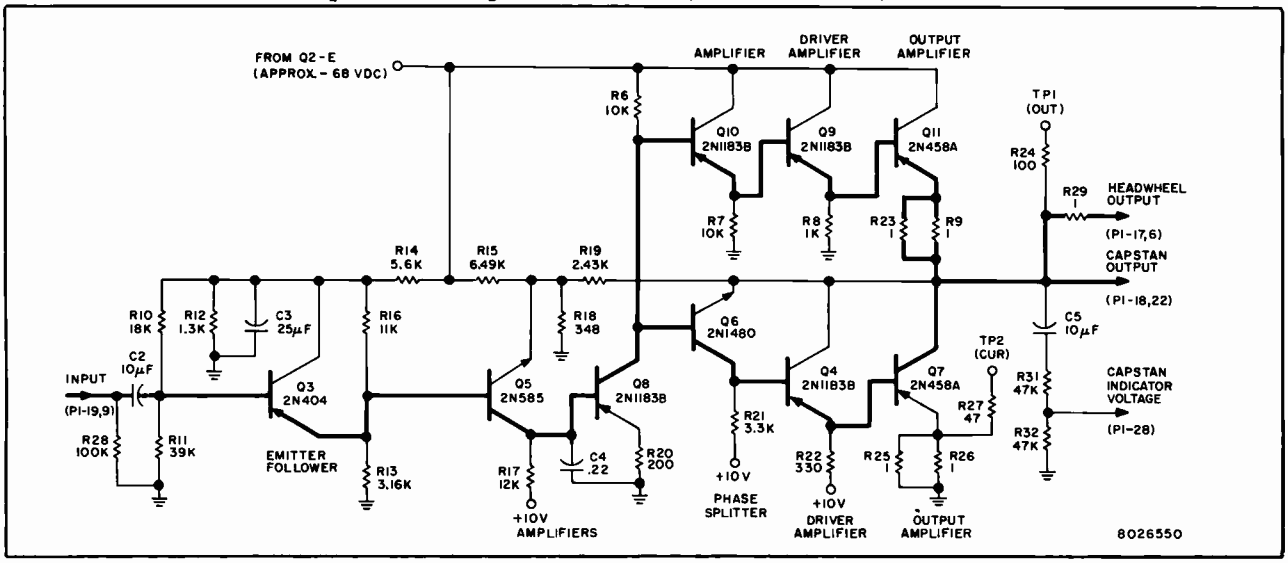


Figure 119—Amplifier Circuits

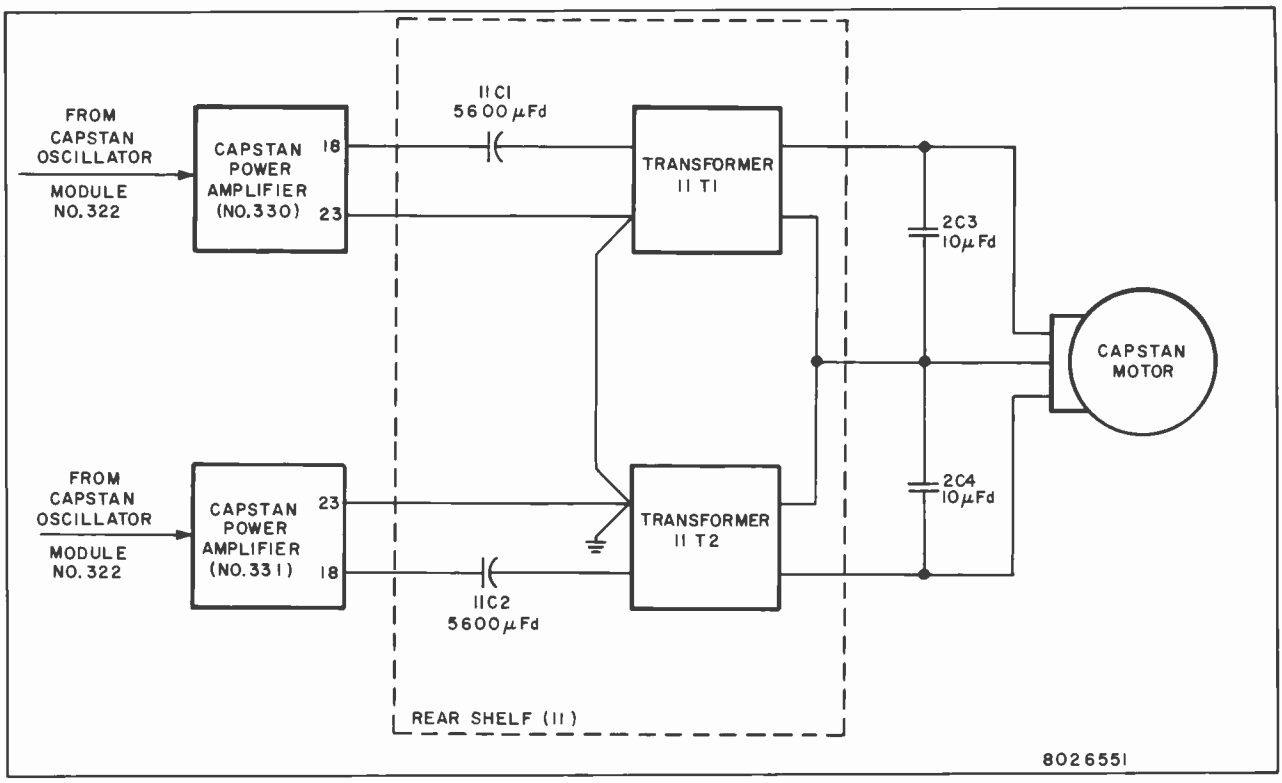
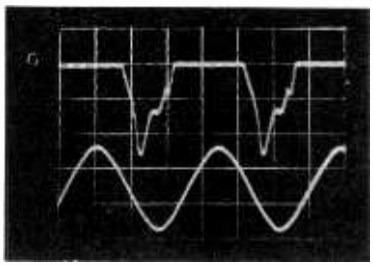
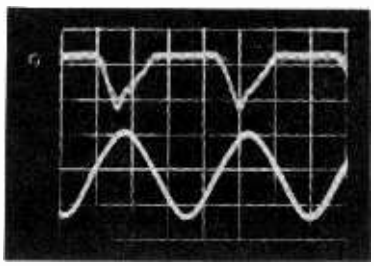


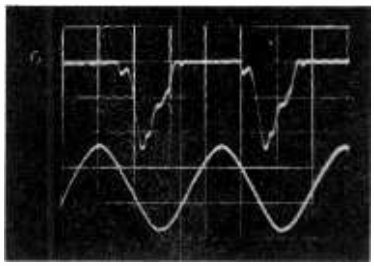
Figure 120—Capstan Power Amplifier and Motor Circuits



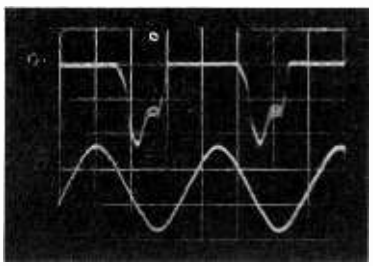
A. Top: TP2 (CUR).
Bottom: TP1 (OUT).
Machine in RECORD mode



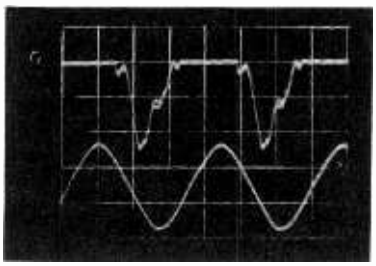
B. Top: TP2, 0.1v/cm.
Bottom: TP1, 20v/cm.
Machine starting up in PLAY/TW mode



C. Top: TP2.
Bottom: TP1.
Machine in PLAY/TW mode



D. Top: TP2.
Bottom: TP1.
Machine in PLAY/SW mode



E. Top: TP2.
Bottom: TP1.
Machine in PLAY/PL mode

All sweep times 5 msec/cm; all amplitudes 0.5v/cm (top) and 20v/cm (bottom), unless otherwise specified.

Figure 121—Capstan Power Amplifier Voltage and Current Output Waveforms

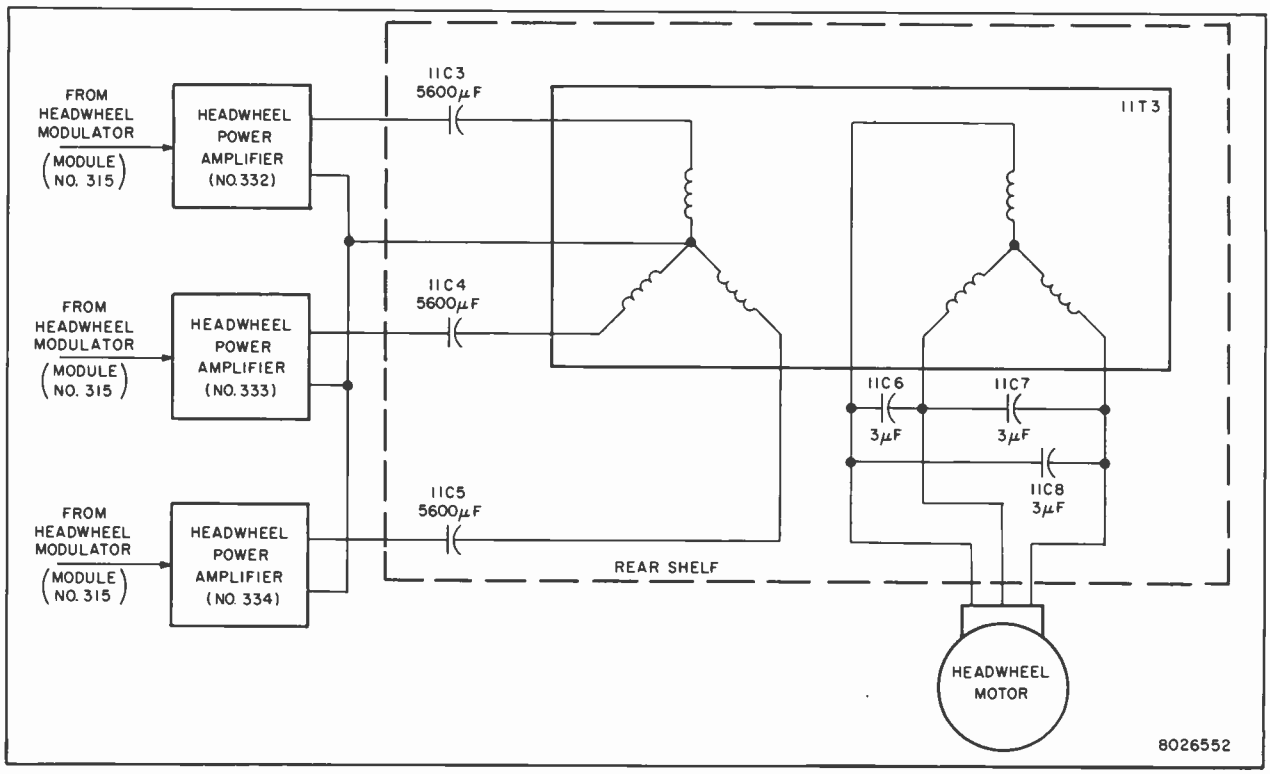
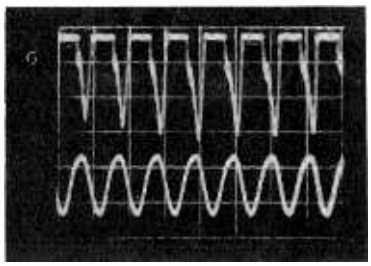
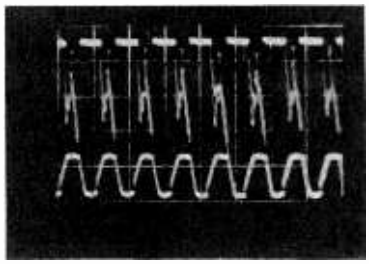


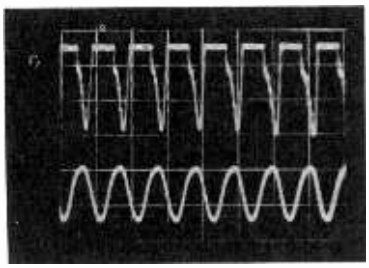
Figure 122—Headwheel Power Amplifier and Motor Circuits



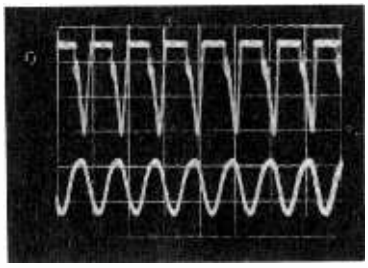
A. Top: TP2 (CUR).
Bottom: TP1 (OUT).
Machine in RECORD mode



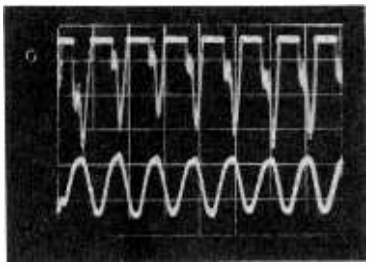
B. Top: TP2, 1v/cm.
Bottom: TP1, 50v/cm.
Machine starting up in PLAY/TW mode



C. Top: TP2.
Bottom: TP1.
Machine in PLAY/TW mode



D. Top: TP2.
Bottom: TP1.
Machine in PLAY/SW mode



E. Top: TP2.
Bottom: TP1.
Machine in PLAY/PL mode

All sweep times 2 msec/cm; all amplitudes 0.1 v/cm (top) and 20 v/cm (bottom), unless otherwise noted.

Figure 123—Headwheel Power Amplifier Voltage and Current Output Waveforms

(5600 microfarads) because of the low transformer and reflected motor impedance. Transformers 11T1 and 11T2 step up the motor voltage to approximately 115 volts rms before it is fed to the capstan motor, and capacitors 2C3 and 2C4 are the capstan motor phase capacitors. Figure 121 shows the waveforms obtained at test points TP2 and TP1 of a capstan power amplifier module during recording and during playback in the switchlock, tonewheel, and pixlock modes of servo operation.

The output voltages from the headwheel power amplifier modules have a frequency of 480 cps and differ in phase by 120 degrees. The voltages are fed through 5600 microfarad electrolytic capacitors 11C3, 11C4, and 11C5, to transformer 11T3 (figure 122). The electrolytic capacitors block the d-c component of the output voltage and couple the 480-cycle output signal to transformer 11T3 and the headwheel motor. Transformer 11T3 steps up the output voltage from the headwheel power amplifier modules to a magnitude which is sufficient to drive the headwheel motor at the correct speed, and capacitors 11C6, 11C7, and 11C8 are the headwheel motor phase capacitors. Figure 123 shows the waveforms obtained at test points TP2 and TP1 of a headwheel power amplifier module during recording and during playback in the tonewheel, switchlock, and pixlock modes of servo operation, as well as during start-up for playback in the tonewheel servo mode.

Capacitor C5 and resistors R31 and R32 form a network which is utilized in obtaining a sampling of the output voltage from the capstan power amplifier modules. The sampled voltage is fed from pin 28 of plug P1 to circuitry in the indicator module (no. 309) which controls the red CAPSTAN warning lamp located above the RECORD control panel. If the output voltage level of either capstan power amplifier drops to a value which is too low for proper servo operation, the indicator module circuitry will cause the CAPSTAN warning lamp to become energized, thus indicating insufficient capstan motor drive.

MAINTENANCE

Trouble in the power amplifier module generally results in a blown fuse, which is indicated by the illumination of the lamp (FUSE IND) on the module front panel. Occasionally a fuse may blow as a result of an overload due to transients; therefore, before checking the module for component failure, turn off machine and replace the blown fuse. If the new fuse blows immediately after the machine has been started up again, trouble in the module circuitry is indicated.

To trouble-shoot the module circuitry rapidly and efficiently, the procedure outlined below should be observed. D-c measurements should be made with a vacuum tube voltmeter such as the RCA Type *WV-98A Voltohmyst*. Test equipment required in making a-c measurements includes a *Tektronix Type 535-A* oscilloscope or the equivalent, and an audio oscillator.

1. Turn off machine, remove module, and check transistors Q2, Q11, and Q7 for collector-to-emitter short circuits.

> *CAUTION: When checking transistors for collector-to-emitter short circuits, use RX100 or RX1000 scale on the ohmmeter.*

2. Replace fuse (3 amp, 3AG) and transistors Q2, Q11, and/or Q7 if found to be shorted.

> NOTE: If transistors Q11 and Q7 continually develop short circuits, driver transistors Q9 and Q4 should be checked for leakage and breakdown characteristics at their maximum rating.

3. Plug module back into machine and turn machine on.

4. If the fuse blows again, proceed as follows:

a. Turn machine off and remove module.

b. Check all transistors for collector-to-emitter short circuits, observing *CAUTION* notation above.

c. Plug module extender into vacant receptacle left by removal of module, turn on machine, and check pin 11 or 21 of extender receptacle for +10 volts dc. If the voltage is not present, trace back utilizing the d-c voltage wiring diagram.

d. If +10 volts dc is obtained at pin 11 or 21 of the extender receptacle and transistor Q11 and/or Q7 has failed, the input stages must be checked.

5. To check the input stages, proceed as follows with the machine turned off and the module removed:

a. Remove transistors Q11 and Q7 from the module.

b. Open the output line by disconnecting wires to pins 17 and 18 of plug P1 at the resistors (not at the plug).

c. Disconnect resistors R7 and R8 from ground, tie the disconnected leads together to form a common lead, and connect a wire from the common lead to the output bus (terminal on block which serves as common collector of transistors Q4 and Q7).

d. Replace fuse.

e. Place module on extender; turn machine on and leave in STOP mode.

f. Check for correct d-c voltages as indicated in the column designated *TEST* in the accompanying *DC VOLTAGE TABLE*.

g. After trouble has been located, replace transistors

Q11 and Q7, and carefully resolder resistors and wires to their original locations.

6. If a-c measurements are to be made, proceed as follows:

a. Turn off machine and remove module.

b. Open the output line by disconnecting wires to pins 17 and 18 of plug P1 at the resistors (not at the plug).

c. Open input by disconnecting the positive (+) lead of capacitor C2.

d. Place the module on an extender and turn machine on in the STOP mode.

e. Adjust the audio oscillator frequency to 60 or 480 cps (or any frequency in between), and adjust the output amplitude to a nominal value of 5.5 volts peak-to-peak.

f. Connect the oscillator to the disconnected lead of capacitor C2 and check the waveforms at each stage.

NOTE: With the output line open there will be no current waveform at test point TP2 (CUR) since no current is drawn by an output load. If it is desired to check the amplifier under full load conditions, a 7½-ohm, 60-watt resistor should be connected between the point where the wire to pin 18 has been removed and ground.

DC VOLTAGE TABLE*

Transistor	*Normal*	*Test*†
Q1 COLLECTOR	−70	−70
Q1 BASE	−70	−70
Q2 COLLECTOR	−70	−70
Q2 BASE	−70	−70
Q3 BASE	−6.7	−6.7
Q3 EMITTER	−6.6	−6.6
Q3 COLLECTOR	−10.5	−10.5
Q5 EMITTER	−6.7	−3.6
Q5 COLLECTOR	−0.9	+9.5
Q8 EMITTER	−0.8	0
Q8 COLLECTOR	−32.5	−70
Q6 EMITTER	−32	−3.5
Q6 COLLECTOR	+8.9	+9.5
Q4 EMITTER	+8.9	+9.5
Q7 EMITTER	0	0
Q10 COLLECTOR	−70	−70
Q10 EMITTER	−32	−70
Q9 EMITTER	−32	−70
Q11 EMITTER	−32	−3.5

* D-c voltages obtained with *RCA Type WV-98A Voltohmyst* using ground as reference. Machine in STOP mode; any power amplifier module.

† See step 5f in the trouble-shooting procedure.

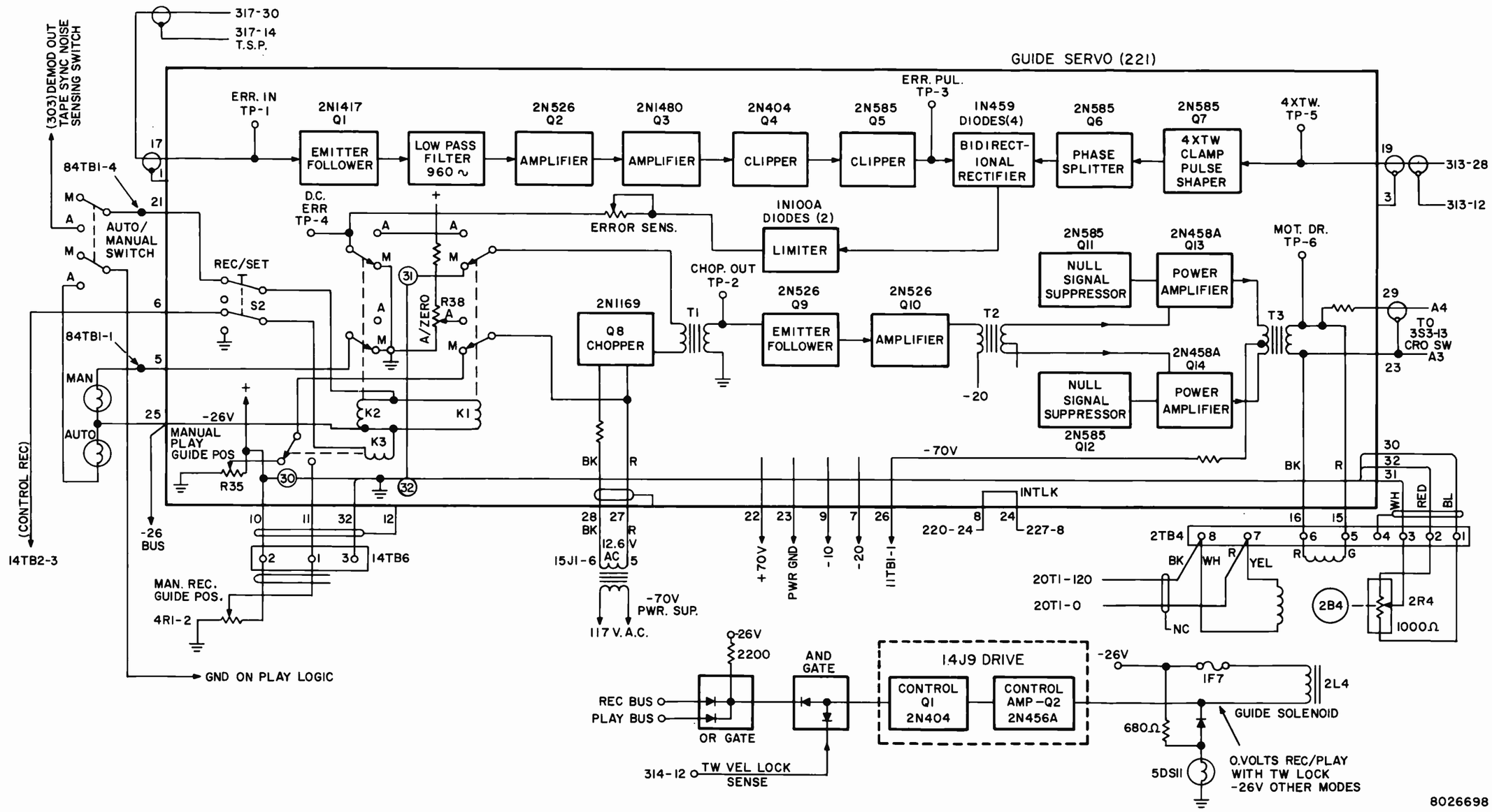


Figure 127—Guide Servo Functional Diagram

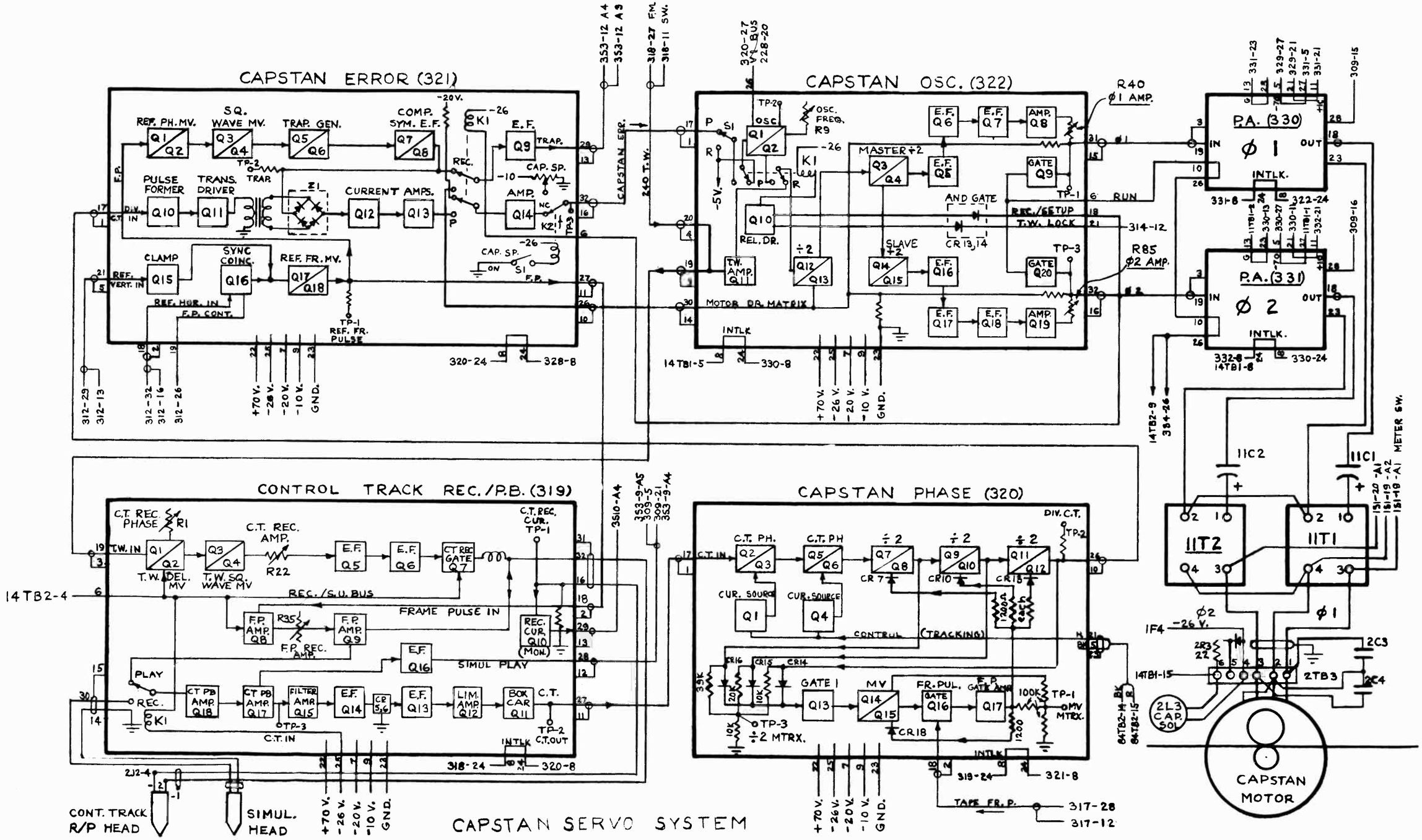


Figure 126—Capstan Servo Functional Diagram

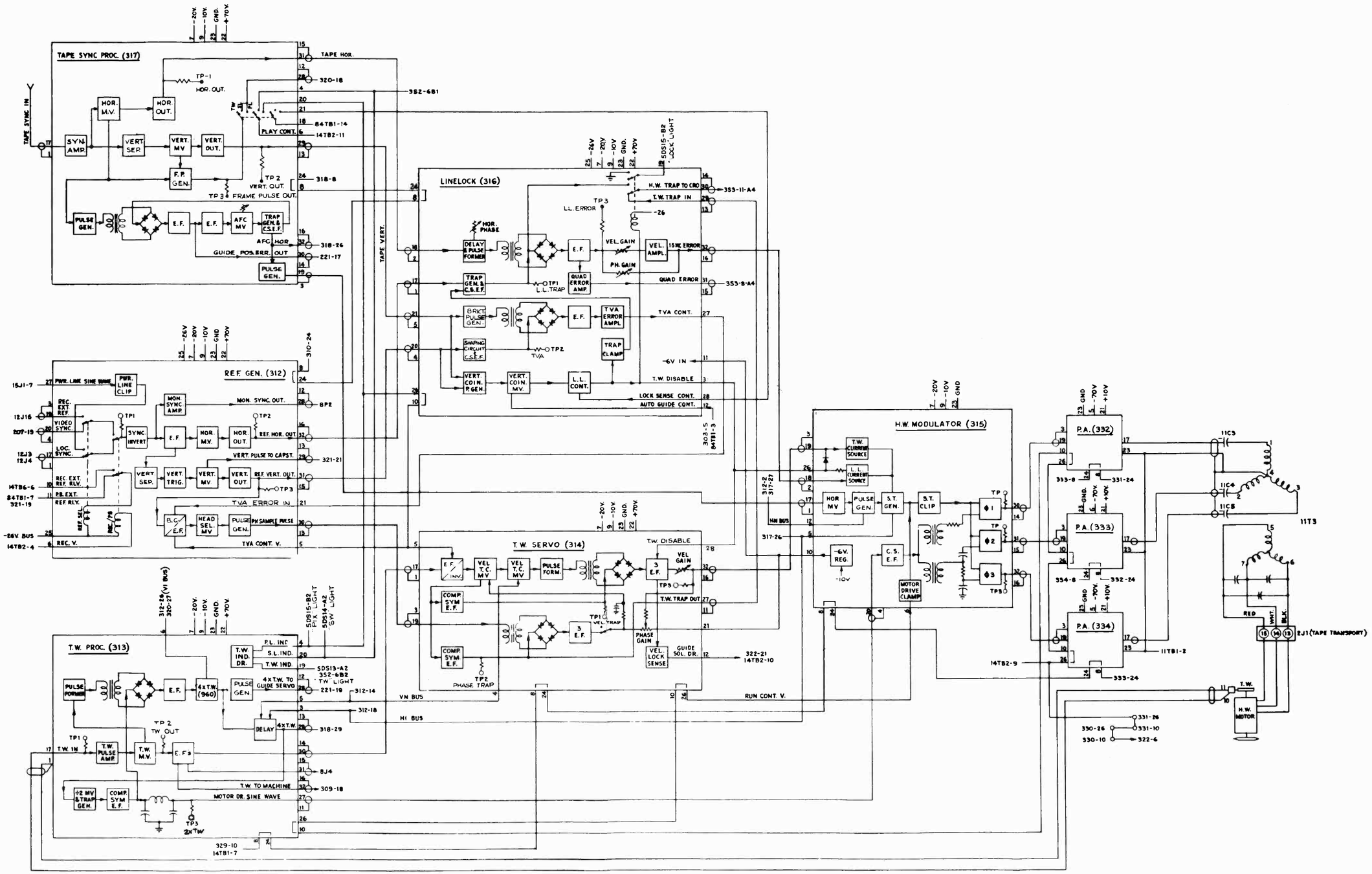


Figure 125—Headwheel Servo Functional Diagram

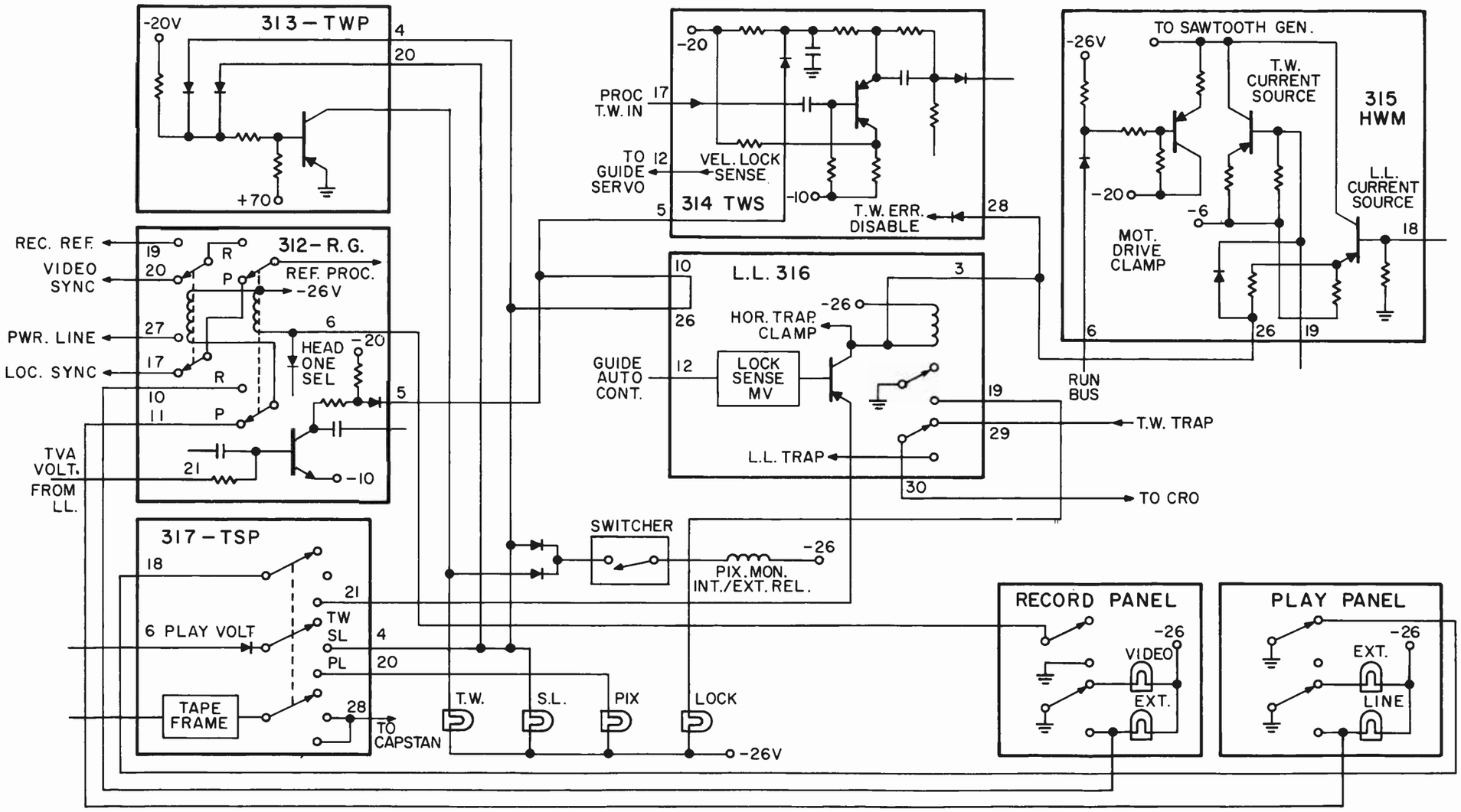


Figure 124—Headwheel Servo Controls and Indicators Diagram

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